**Hyperspectral image lossy compression on a reconfigurable and fault-tolerant architecture implemented over a COTS FPGA-based SoC**

The use of hyperspectral sensors on-board the satellites is considered essential for environmental studies. Current space missions are incorporating this kind of sensors and there is a tendency to include them in missions to analyse cosmic bodies, such as the Moon surface or Mars, mainly with identification and detection purposes. The acquired images from these sensors are big in terms of memory occupation and it is difficult to send them directly to the ground stations due to bandwidth limitations. Therefore, it is necessary to apply compression techniques on-board the satellites before sending them to the Earth surface, in order to reduce their volume.

In the other hand, Field Programmable Gate Arrays (FPGAs) have been used more and more for space applications due to their reprogrammable capabilities, good performance, low power consumption and cost reduction compare to ASICs. Although there are available in the market Rad-Hard By Design (RHBD) FPGAs specifically designed for space missions, at present the use of Commercial Off-The-Shelf (COTS) SRAM-based FPGAs is becoming interesting due to their greater performance in comparison with RHBD devices. Usually these FPGAs are combined with microprocessors in the same die, forming heterogeneous System-on-Chip (SoC) that increases the capabilities of the system in terms of computational operation without compromising its power consumption. However, this technology is vulnerable to radiation in space environments, which can cause errors in the configuration memory deriving in an incorrect operation of the system or even in its total failure. Nevertheless, a number of techniques, such as scrubbing and redundancy, are currently available to prevent or mitigate the radiation effects in order to preserve the data integrity and system functionality.

Regarding FPGA design, it is usually tackled at Register Transfer Level (RTL) but with the increase of the system complexity is necessary to use a methodology that allows to reduce both the design process and the Time-To-Market (TTM). In this way, a High-Level Synthesis methodology (HLS) approach can be used, starting from an algorithmic model in C/C++ language that is automatically transform by HLS tools in its equivalent RTL description.

This work presents an implementation of a lossy extension of the CCSDS (Consultative Committee for Space Data Systems) 123.0-B-1 lossless standard, specifically thought for multispectral and hyperspectral images. This standard is intended for space applications, looking for a trade-off between its compression efficiency and the design complexity. The proposed lossy extension includes a bit rate control to define the losses the compressor must introduce in order to achieve higher compression ratios without compromising the relevant image information. To complete the design flow, an HLS methodology has been followed. This system is implemented over a reconfigurable and fault-tolerant architecture, named ARTICo$^3$, developed by the Universidad Politécnica de Madrid (UPM) and specially thought for space applications, including scrubbing and redundant techniques, such as Double and Triple Modular Redundancy (DMR and TMR, respectively), in critical parts of the FPGA fabric. The proposed solution is able to adapt the system operation taking into account different features, such as the computational performance, the power consumption or the robustness against faults. The reconfiguration engine runs on an ARM with embedded Linux OS. The system has been tested on both a Xilinx Zynq XC7Z020 and a Zynq UltraScale+ XCZU9EG, obtaining different results in terms of speed up depending on the number of hardware accelerators implemented on the ARTICo$^3$ architecture. The results of this work have been obtained in a European funded project called ENABLE-S3, where ULPGC and UPM are partners in the aerospace use case.