A Simple Method to Extract the Thermal Resistance of GaN HEMTs from De-trapping Characteristics

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***Abstract*— This paper proposes a new method for extracting the thermal resistance of GaN-based HEMTs using pulse recovery data. After the device temperature and trapping state are established from different quiescent power dissipations for several base-plate temperatures, the recovery profile of the drain current is measured. The recovery time is then used as a temperature-sensitive electrical parameter to extract the thermal resistance of the device. The proposed method has been applied to a Schottky-gate HEMT on SiC, for which a thermal resistance of 15.7 °C-mm/W was extracted, a value in good agreement with others reported for similar devices. Comparison with the one obtained from a step response is also done. Finally, the uncertainties of the proposed method related to the pulse width, temperature, percentage of the drain current recovery time, and averaging procedure are discussed.**

***Index Terms*— pulse recovery data, electrothermal characterization, trapping, gallium nitride, high-electron-mobility transistors (HEMTs), thermal resistance.**

I. Introduction

THERE are several techniques for measuring the thermal resistance, R_{th}, of GaN high-electron mobility transistors (HEMTs), such as pulsed characteristics [1], [2], step response [3], infrared and Raman thermography [4], [5], and AC conductance method [6]. Temperature-sensitive electrical parameters (TSEPs), such as the forward voltage drop between the gate and source [7], the channel ON-resistance [7], [8], the saturation drain current [9], and the gate metal resistance [10], [11], have also been used to extract the R_{th} of HEMTs. Limitations of all these techniques are addressed in [6].

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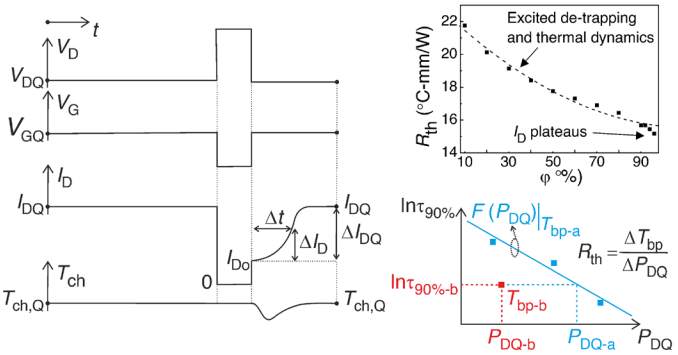

Fig. 1. Illustration of the pulse response method: the excitation waveforms and the drain current with the de-trapping recovery phenomenon and the respective channel temperature variation, together with $R_{th\text{-}\varphi}$ vs. φ, and the extraction of R_{th} with the VFM.

Knowing that the de-trapping time is very sensitive to temperature (one order of magnitude for a 40 °C swing) [12]–[17], the main objective of this work is to take advantage of this feature and develop a simple and fast but precise thermo-electrical method, using easily accessible equipment in most RF laboratories, to extract the thermal resistance of HEMTs from pulse recovery data. Moreover, contrary to other simpler methodologies [1]–[3], [6], [8], [9], the proposed method does not require any separation of thermal and trapping effects. It can be applied to extract the thermal resistance of packaged devices, by simply mounting them on thermal stages and automatically repeating the procedure.

The method is described in Section II. The experimental setup and the characteristics of the tested device are detailed in Section III. The results and experimental validation are presented in Section IV. Conclusions are given in Section V.

II. Proposed Technique

The new method to extract the R_{th} of GaN HEMTs is based on the dependence of the de-trapping time constant on the channel temperature, T_{ch}. As shown in Fig. 1, after setting the base-plate temperature, T_{bp}, the measurement sequence starts by setting different quiescent gate- and drain-source voltages, V_{GQ} and V_{DQ}, respectively, to generate a quiescent drain current, I_{DQ}, and to consequently increase T_{ch}. The initial biasing period should be sufficiently long (around 5 min) to ensure a steady-state condition, with $T_{ch} = T_{ch,Q}$. A high drain voltage, V_D, is then applied to induce charge trapping, while the gate voltage, V_G, is simultaneously pulsed down to avoid

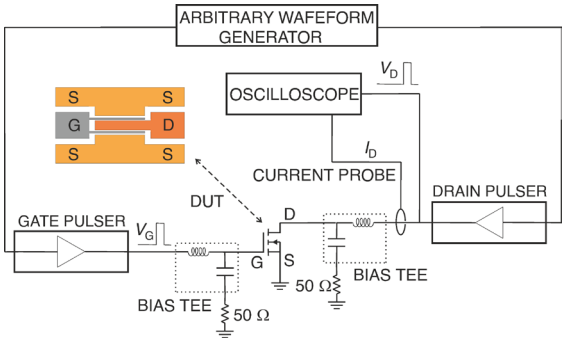

Fig. 2. Diagram of the experimental setup.

temperature spikes. These pulses must be narrow enough (1 µs) to prevent a significant decrease of T_{ch}, while, at the same time, ensuring considerable trapping. With this, we can assume that, immediately after the pulse is stepped down, right when the de-trapping process is about to start, $T_{ch} \approx T_{ch,Q}$.

During the de-trapping process, the drain current, I_D, recovers from an initial value, I_{Do}, to I_{DQ}, where the channel temperature is again $T_{ch,Q}$. Thus, with a percentage of $I_{DQ} - I_o$, φ, as a criterion, the drain current recovery time, τ_φ, given by:

$$\tau_\varphi\,(T_{ch,Q}) = \Delta t\big|_{\frac{\Delta I_D}{\Delta I_{DQ}} = \frac{\varphi}{100}} = \Delta t\big|_{\frac{I_D - I_{Do}}{I_{DQ} - I_{Do}} = \frac{\varphi}{100}} \quad (1)$$

could be used as a TSEP with $T_{ch,Q}$ (see Fig. 1).

The de-trapping process can be physically described by the Shockley-Read-Hall model, where the emission time constant, τ_e, is given by $A^{-1}T_{ch}^{-2}\exp(E_A/(K_B T_{ch}))$, with E_A and K_B being the trap activation energy and Boltzmann constant, respectively, and A incorporates the remaining temperature independent parameters [18]. In a steady-state regime, τ_φ in (1) is directly proportional to τ_e. Then, considering a small range of channel temperature variation (typically 40 °C of variation), $\delta T_{ch} = \delta T_{bp} + R_{th} \times \delta P_{DQ}$, with $P_{DQ} = I_{DQ}V_{DQ}$ being the quiescent power dissipation, $\ln\tau_\varphi$ can be easily linearized without significantly increasing the error. That is,

$$\ln\tau_\varphi \approx a_o - a_1 \times T_{chQ} \approx a_o - a_1 \times (T_{bp} + R_{th} \times P_{DQ}) \quad (2)$$

where a_o and a_1 are fitting parameters that can be extracted using least squares to minimize the mean quadratic error with respect to the measured data. The accuracy of this method lies in the use of multiple base-plate temperatures and power dissipations, resulting in an average R_{th}. Additionally, R_{th} could be extracted for a wide range of T_{ch} (varying T_{bp} and P_{DQ}), by dividing it into small consecutive ranges for which $\ln\tau_\varphi$ can be linearized.

In our case, during the pulse, and certainly during the de-trapping process, some thermal dynamics can be excited, which leads the slight decrease of T_{ch}, as it is illustrated in Fig. 1. Nevertheless, for high percentages of the drain current recovery time, T_{ch} tends to the original value, T_{chQ}, imposed by $T_{bp} + R_{th} \times P_{DQ}$, when (2) is valid. As Fig. 1 shows, where the dependence of the extracted thermal resistance on φ is represented (measured data with solid squares and their trend with a dashed line), a percentage of between 90–95% turns out to be reasonable. For $\varphi < 90\%$, an unrealistic overestimated R_{th} would be obtained due to excited de-trapping and thermal dynamics and, for φ at nearly 100%, I_D tends to plateau and

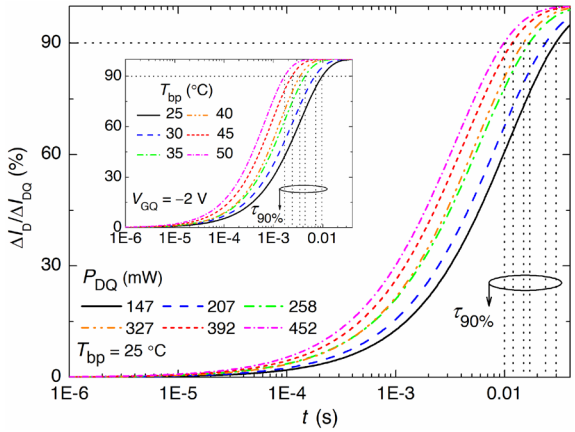

Fig. 3. Percentage of the recovered drain current (lines) vs. recovery time, for different P_{DQ} and T_{bp} = 25 °C. The inset shows analogously the same dependency for different T_{bp} with V_{GQ} = –2 V. In both cases, the 90% criterion for the drain current recovery time is indicated with horizontal and vertical lines.

the uncertainty in the extracted recovery time increases.

In [19] a simple thermally activated trapping model based on SRH model was proposed. In this model, the trapping dynamics induces a threshold voltage shift is modeled by the charging (for capture) and discharging (for emission) of a capacitor through the corresponding R-C linear system. By incorporating self-heating effects using a first-order thermal network, as in [13] and [19], the proposed method could be reproduced without a significant deviation of the extracted R_{th} from the thermal network, showing its consistency.

Alternatively, as Fig. 1 shows, a linear relationship, F, between $\ln\tau_{90\%}$ and P_{DQ} can be extracted for a base-plate temperature $T_{bp\text{-}a}$ (with, at least, three quiescent power dissipations). Then, for a given pair of [$T_{bp\text{-}b}$, $P_{DQ\text{-}b}$] with $\tau_{90\%\text{-}b}$, the necessary quiescent power dissipation for producing the same channel temperature at $T_{bp\text{-}a}$ results in $P_{DQ\text{-}a} = F^{-1}(\ln\tau_{90\%\text{-}b})$. Since [$T_{bp\text{-}a}$, $P_{DQ\text{-}a}$] and [$T_{bp\text{-}b}$, $P_{DQ\text{-}b}$] follow (2) with $\tau_{90\%\text{-}b}$, R_{th} results $(T_{bp\text{-}a} - T_{bp\text{-}b})/(P_{DQ\text{-}b} - P_{DQ\text{-}a}) = \Delta T_{bp}/\Delta P_{DQ}$. This will be named a very fast method (VFM).

III. Experimental Setup

A diagram of the experimental setup is shown in Fig. 2, with an arbitrary waveform generator (Tektronix AWG5012C) generating the gate and drain voltage pulses, which were then amplified using two pulser heads and bias-tees (Keysight 11612A) to prevent possible oscillations at high frequencies. The drain current was obtained through a 120-MHz bandwidth Hall-effect current sensor (TCP0030A) connected to a high-speed digital oscilloscope (Tektronix DPO3052) [18], and the bare die was placed directly on a hotplate to maintain T_{bp} in the range 25−50 °C, with steps of 5 °C.

A GaN Schottky-gate HEMT on SiC with a threshold voltage of −3 V, a gate length of 0.25 µm, and a gate width of 400 µm (2 × 200 µm) was used to validate the method.

Since the gate-lag phenomenon is nowadays solved [20]–[22], to generate different P_{DQ} without changing the trapping state, only the quiescent gate voltage, V_{GQ}, is changed from –2.5 to –2 V in steps of 0.1 V and the V_{DQ} if fixed at 6 V. Short-pulsed voltages of 40 and –5 V for the drain and gate terminals, respectively, induced the current collapse.

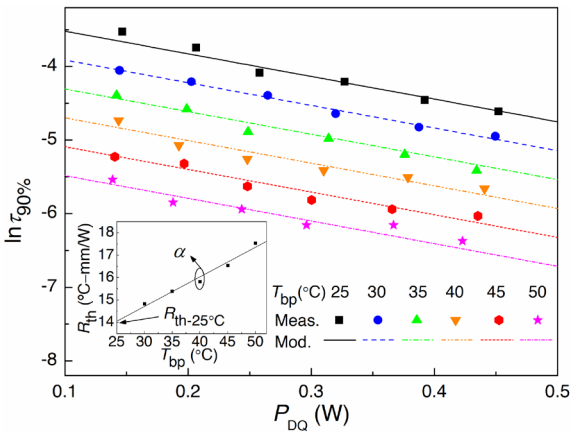

Fig. 4. 90% of the drain current recovery time vs. power dissipation, at different base-plate temperatures. The inset shows the linear temperature dependence of R_{th} with the VFM. Measured and modeled data are represented by symbols and lines, respectively.

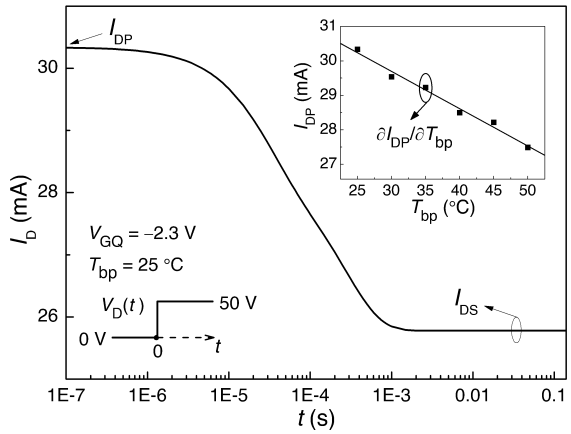

Fig. 5. Drain current response to a positive drain voltage step of 50 V with V_{GQ} = –2.3 V and T_{bp} = 25 °C. The inset shows the linear base-plate temperature dependence of the peak drain current, I_{DP}.

IV. Results and Validation

Fig. 3 shows the percentage of the recovered I_D (with lines) after the pulsed OFF-state stress for a base-plate temperature of 25 °C at different quiescent power dissipations. The corresponding 90% of the drain current recovery time, $\tau_{90\%}$, is indicated with vertical lines. As expected from (2), the higher the quiescent power dissipation, the sooner the drain current recovers due to enhanced self-heating effects. The inset in Fig. 3 shows similarly the recovery dynamics of the drain current and $\tau_{90\%}$ at different base-plate temperatures for a representative quiescent gate voltage of V_{GQ} = –2 V. Naturally, a faster recovery is observed when the base-plate temperature is increased as described by (2).

The resulting quiescent power dissipation dependence of the 90% of the normalized drain current recovery time, $\ln \tau_{90\%}$, is shown in Fig. 4 with symbols for each base-plate temperature. By applying (2) and considering all base-plate temperatures and power dissipations, the extracted values for a_o, a_1, and R_{th} are –1.25, 0.08 °C^{-1}, and 15.7 °C-mm/W, respectively. The resulting modeled data for $\ln \tau_{90\%}$ are shown in Fig. 4 with lines, showing a good agreement with the measurements with an average relative error of 6.3%.

Because the R_{th} of HEMTs depends on the gate length [2], [6], our result (15.7 °C-mm/W) has been compared with data reported for 0.25 µm GaN-based HEMTs on SiC: 18.3 and 12.6 °C-mm/W in [2] and [8], respectively, using pulse response measurements and the channel ON-resistance as TSEP, and 15.5 °C-mm/W in [3] using a step response, which shows that our result is in same range. A more specific comparison would require the use of the same power densities and even transistors with similar gate-to-drain extension [23].

The R_{th} in our device was also measured by making use of the step response technique [3]. Fig. 5 shows the resulting drain current transient response affected only by self-heating and measured for a V_D step of 50 V with a fixed V_{GQ} = –2.3 V and T_{bp} = 25 °C; it can be seen that I_D decreases with a thermal time constant, τ_{th}, of ~100 μs. The inset shows the linear base-plate temperature dependence of the peak drain current, without self-heating, I_{DP}. So $R_{th} = (I_{DS} - I_{DP})/(P_{DS} \times \partial I_{DP}/\partial T_{bp})$, using the stationary power dissipation $P_{DS} = V_D \cdot I_{DS}$, resulting in 13.1 °C-mm/W, which is in good agreement with that obtained with the new method.

For the new method, with a pulse width, PW, of 1 µs, the normalized temperature rise, $\Delta T_{ch}/\Delta T_{chQ}$, with $\Delta T_{ch} = T_{ch} - T_{bp}$, results in $\exp(-PW/\tau_{th}) > 0.99$ at the end of the pulse. Thus, the initial and final T_{ch} of the de-trapping process match. Otherwise, the method is not valid since $\tau_{90\%}$ is overvalued and R_{th} is undervalued. So the smaller the τ_{th} the narrower the required PW, particularly when 3-D heat spreading creates a broad time constant spectrum [24]. Once a valid PW is set for a significant P_{DQ} and T_{bp} pair, the PW would remain valid at higher P_{DQ} and T_{bp} values since τ_{th} would increase [25].

The difference between the R_{th} values extracted by the two methods could relate to where the temperature is being perceived [17]. For both electrothermal methods, the temperature is averaged in the device channel, with the proposed one also perceiving where traps are located. Thus, R_{th} values extracted with the proposed method might be overvalued or undervalued if $\tau_{90\%}$ refers to a trap located close to the hot spot in the device or far away from it, respectively.

Finally, assuming a linear temperature dependence for the thermal resistance, $R_{th} \approx R_{th\text{-}25°C}\,[1 + \alpha\,(T_{bp} - 25)]$, by applying the VFM with $T_{bp\text{-}a}$ = 25 °C and $P_{DQ\text{-}b} = \langle P_{DQ\text{-}a} \rangle$ (~ 0.25 W), varying $T_{bp\text{-}b}$, $R_{th\text{-}25°C}$ results 14.1 °C-mm/W and a temperature coefficient α of 0.009 °C^{-1} is predicted, in agreement with [3]. The inset in Fig. 4 shows the modeled data for R_{th} with a line. However, by using the VFM with the role of T_{bp} and P_{DQ} swapped, no linear dependence of R_{th} on P_{DQ} is achieved [26], which is attributed to the low power densities used [27].

V. Conclusion

A fast, highly sensitive and simple thermo-electrical method for any standard testing laboratory, to extract the thermal resistance of GaN-based HEMTs (even packaged devices), has been presented in detail. By obtaining the drain current recovery time for a Schottky-gate HEMT on SiC induced by de-trapping for different power dissipations and base-plate temperatures, the thermal resistance of the device, including the temperature dependence, has been determined. A good agreement with other reported data and the thermal resistance measured with the step response technique has been achieved.

REFERENCES

[1] V. I. Smirnov, V. Sergeev, A. Gavrikov, and A. Kulikov, "Measuring thermal resistance of GaN HEMTs using modulation method," *IEEE Trans. Electron Devices*, vol. 67, no. 10, pp. 4112–4117, Oct. 2020, doi: 10.1109/TED.2020.3013509.

[2] J. Joh, J. A. del Alamo, U. Chowdhury, T.-M. Chou, H.-Q. Tserng, and J. L. Jimenez, "Measurement of channel temperature in GaN high electron mobility transistors," *IEEE Trans. Electron Devices*, vol. 56, no. 12, pp. 2895–2901, Dec. 2009, doi: 10.1109/TED.2009.2032614.

[3] C. Florian, A. Santarelli, R. Cignani, and F. Filicori, "Characterization of the nonlinear thermal resistance and pulsed thermal dynamic behavior of AlGaN–GaN HEMTs on SiC," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 5, pp. 1879–1891, May 2013, doi: 10.1109/TMTT.2013.2256146.

[4] L. Baczkowski, J. Jacquet, O. Jardel, C. Gaquière, M. Moreau, D. Carisetti, L. Brunel, F. Vouzelaud, and Y. Mancuso, "Thermal Characterization Using Optical Methods of AlGaN/GaN HEMTs on SiC Substrate in RF Operating Conditions," *IEEE Trans. Electron Devices*, vol. 62, no. 12, pp. 3992–3998, Dec. 2015, doi: 10.1109/TED.2015..

[5] M. Kuball and J. W. Pomeroy, "A review of Raman thermography for electronic and opto-electronic device measurement with submicron spatial and nanosecond temporal resolution," *IEEE Trans. Device Mater. Rel.*, vol. 16, no. 4, pp. 667–684, Dec. 2016, doi: 10.1109/TDMR.2016.2617458.

[6] B. González, A. Lázaro, and R. Rodríguez, "RF extraction of thermal resistance for GaN HEMTs on Silicon," *IEEE Trans. Electron Devices*, vol. 69, no. 5, pp. 2307–2312, May 2022, doi: 10.1109/TED.2022.3159611.

[7] Y. Shan, W. Gao, Z. Huang, W. Kuang, Z. Wu, and B. Zhang, "Test methods and principles of thermal resistance for GaN HEMT power devices," in *Proc. 21st Int. Conf. Electron. Packag. Technol. (ICEPT)*, Guangzhou Science City, China, Aug. 2020, pp. 1–4, doi: 10.1109/ICEPT50128.2020.9202571.

[8] R. Sommet, G. Mouginot, R. Quere, Z. Ouarch, and M. Camiade, "Thermal modeling and measurements of AlGaN/GaN HEMTs including thermal boundary resistance," *Microelectron. J.*, vol. 43, no. 9, pp. 611–617, Sep. 2012, doi: 10.1016/j.mejo.2011.07.009.

[9] J. Kuzmik, R. Javorka, A. Alam, M. Marso, M. Heuken, and P. Kordos, "Determination of channel temperature in AlGaN/GaN HEMTs grown on sapphire and silicon substrates using DC characterization method," *IEEE Trans. Electron Devices*, vol. 49, no. 8, pp. 1496–1498, Aug. 2002, doi: 10.1109/TED.2002.801430.

[10] B. K. Schwitter, A. E. Parker, A. P. Fattorini, S. J. Mahon, and M. C. Heimlich, "Study of gate junction temperature in GaAs pHEMTs using gate metal resistance thermometry," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3358–3364, Oct. 2013, doi: 10.1109/TED.2013.2278704.

[11] G. Pavlidis, S. Pavlidis, E. R. Heller, E. A. Moore, R. Vetury, and S. Graham, "Characterization of AlGaN/GaN HEMTs using gate resistance thermometry," *IEEE Trans. Electron Devices*, vol. 64, no. 1, pp. 78–83, Jan. 2017, doi: 10.1109/TED.2016.2625264.

[12] Y. Gu, W. Huang, Y. Zhang, J. Sui, Y. Wang, H. Guo, J. Zhou, B. Chen, and X. Zou, "Temperature-Dependent Dynamic Performance of p-GaN Gate HEMT on Si," *IEEE Trans. Electron Devices*, vol. 69, no. 6, pp. 3302–3309, Jun. 2022, doi: 10.1109/TED.2022.3167342.

[13] J. L. Gomes, L. C. Nunes, F. M. Barradas, A. Cooman, A. E. F. de Jong, R. M. Heeres, and J. C. Pedro, "The impact of long-term memory effects on the linearizability of GaN HEMT-based power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 70, no. 2, pp. 1377–1390, Feb. 2022, doi: 10.1109/TMTT.2021.3132930.

[14] F. Li, R. Wang, H. Huang, Y. Ren, Z. Liang, G. Ren, P. Tao, Z. Sun, N. Sun, C. Zhao, and H. Liang, "Temperature-dependent hot electron effects and degradation mechanisms in 650-V GaN-based MIS-HEMT power devices under hard switching operations," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 9, no. 5, pp. 6424–6431, Oct. 2021, doi: 10.1109/JESTPE.2021.3061570.

[15] S. Mehari, A. Gavrilov, M. Eizenberg and D. Ritter, "Identification of energy and spatial location of electron traps in AlGaN/GaN HFET structures," *IEEE Trans. Electron Devices*, vol. 64, no. 4, pp. 1642–1646, Apr. 2017, doi: 10.1109/TED.2017.2661960.

[16] M. Meneghini, A. Tajalli, P. Moens, A. Banerjee, E. Zanoni, and G. Meneghesso, "Trapping phenomena and degradation mechanisms in GaN-based power HEMTs," *Mater. Sci. Semicond. Process*, vol. 78, pp. 118–126, May 2018, doi: 10.1016/j.mssp.2017.10.009.

[17] A. Chini, F. Soci, M. Meneghini, G. Meneghesso, and E. Zanoni, "Deep levels characterization in GaN HEMTs—Part II: Experimental and numerical evaluation of self-heating effects on the extraction of traps activation energy," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3166–3182, Oct. 2013, doi: 10.1109/TED.2013.2278290.

[18] J. L. Gomes, L. C. Nunes, C. F. Gonçalves, and J. C. Pedro, "An Accurate Characterization of Capture Time Constants in GaN HEMTs," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 7, pp. 2465–2474, Jul. 2019, doi: 10.1109/TMTT.2019.2921338.

[19] L. C. Nunes, J. L. Gomes, F. M. Barradas and J. C. Pedro, "A simple thermally activated trapping model for AlGaN/GaN HEMTs," in *Proc. 17th European Microw. Integr. Circuits Conf. (EuMIC)*, Milan, Italy, Sep. 2022, pp. 137–140, doi: 10.23919/EuMIC54520.2022.9923433.

[20] L. C. Nunes, J. M. Gomes, P. M. Cabral, and J. C. Pedro, "A new nonlinear model extraction methodology for GaN HEMTs subject to trapping effects," in *Proc. IEEE MTT-S Int. Microw. Symp.*, Phoenix, AZ, USA, May 2015, pp. 1–4, doi: 10.1109/MWSYM.2015.7166977.

[21] O. Jardel, F. De Groote, T. Reveyrand, J.-C. Jacquet, C. Charbonniaud, J.-P. Teyssier, D. Floriot, and R. Quéré, "An electrothermal model for AlGaN/GaN power HEMTs including trapping effects to improve large-signal simulation results on high VSWR," *IEEE Trans. Microw. Theory Techn.*, vol. 55, no. 12, pp. 2660–2669, Dec. 2007, doi: 10.1109/TMTT.2007.907141.

[22] J. L. Gomes, L. C. Nunes, and J. C. Pedro, "Explaining the different time constants extracted from low frequency Y_{22} and I_{DS}-DLTS on GaN HEMTs," in *Proc. IEEE MTT-S Int. Microw. Symp.*, Los Angeles, CA, USA, Aug. 2020, pp. 432–435, doi: 10.1109/IMS30576.2020.9223822.

[23] B. González, C. De Santi, F. Rampazzo, M. Meneghini, A. Nunez, E. Zanoni, and G. Meneghesso, "Geometric modeling of thermal resistance in GaN HEMTs on silicon," *IEEE Trans. Electron Devices*, vol. 67, no. 12, pp. 5408–5414, Dec. 2020, doi: 10.1109/TED.2020.3028358.

[24] K. R. Bagnall, O. I. Saadat, S. Joglekar, T. Palacios, and E. N. Wang, "Experimental Characterization of the Thermal Time Constants of GaN HEMTs Via Micro-Raman Thermometry," *IEEE Trans. Electron Devices*, vol. 64, no. 5, pp. 2121–2128, May 2017, doi: 10.1109/TED.2017.2679978.

[25] K. R. Bagnall and E. N. Wang, "Theory of Thermal Time Constants in GaN High-Electron-Mobility Transistors," *IEEE Trans. Compon. Pack. Manuf. Technol.*, vol. 8, no. 4, pp. 606–620, Apr. 2018, doi: 10.1109/TCPMT.2017.2773065.

[26] J. Liu, L. Sun, Z. Yu, and M. Condon, "A simple method to determine power-dissipation dependent thermal resistance for GaN HEMTs," in *Proc. IEEE MTT-S Int. Microw. Symp.*, Baltimore, MD, USA, Jun. 2011, pp. 1–4, doi: 10.1109/MWSYM.2011.5972752.

[27] J. Bremer, D. Y. Chen , A. Malko, M. Madel, N. Rorsman, S. E. Gunnarsson, K. Andersson, T. M. J. Nilsson, P. E. Raad, P. L. Komarov, T. L. Sandy, and M. Thorsell, "Electric-based thermal characterization of GaN technologies affected by trapping effects," *IEEE Trans. Electron Devices*, vol. 67, no. 5, pp. 1952–1958, May 2020, doi: 10.1109/TED.2020.2983277.