# Gate Geometry-Dependent Thermal Impedance of Depletion Mode HEMTs

Benito González, Antonio Lazaro, *Senior Member, IEEE*, and Raúl Rodríguez

***Abstract*— Although the steady-state thermal behavior of GaN-based high-electron mobility transistors (HEMTs) has been studied extensively, significantly fewer studies have considered their thermal capacitance. In this article, frequency domain characterization has been employed to extract the thermal impedance of GaN depletion mode HEMTs (D-HEMTs) by using an impedance analyzer. The resulting thermal impedances, when varying the channel length and gate width, are successfully modeled for a frequency domain analysis. A conventional fifth-order geometry-dependent thermal network is proposed for a time domain analysis. Thus, this article presents an experimental tool for determining the gate geometry-dependent thermal resistances and capacitances of D-HEMTs for electrothermal modeling. The thermal resistances are comparable to those obtained with pulsed measurements.**

*Index Terms*—**Thermal impedance, electrothermal characterization, gallium nitride, high-electron mobility transistors (HEMTs), AC measurement.**

## I. Introduction

SIGNIFICANT heat generation in the channel of GaN-based high-electron mobility transistors (HEMTs) is one of the main causes for their performance degradation. Accurate characterization and modeling of transistor thermal impedance is, therefore, of paramount importance to most circuit designs [1]–[3].

The steady-state thermal behavior of GaN-based HEMTs has been studied extensively. Several electrothermal techniques have been used for measuring their thermal resistance, such as pulsed characteristics [4], step response [5], and the AC conductance method [6]. Temperature-sensitive electrical parameters (TSEPs), such as the saturation drain current [7], have also been employed. Since measurement techniques based on electrical characterization average the temperature in the active channel area, the extracted thermal resistance predicts a device temperature lower than the peak value (located at the border of the gate by the drain side). However, this is necessary for compact modeling where average temperatures are considered. On other hand, IR and Raman thermographs [8], [9] can determine the temperature of the hot spot in the device. Nevertheless, the former is inaccurate when measuring devices with micrometer or sub-micrometer scale feature sizes, and the latter is limited by the measurement device areas where optical access is not blocked by metal contacts.

Significantly fewer studies have been devoted to the extraction of the thermal capacitance of GaN-based HEMTs. The step response method was used in [5], without considering the trapping state variation with temperature [10]. Alternatively, in [9], by using the step response via micro-Raman thermometry, the thermal time constant spectrum was derived for a high-order *RC* Foster thermal network, which requires elaborated adjustment processes and a high computational cost in circuit design.

In this paper, by using the auto-balancing bridge method [11], the thermal impedance of GaN-based HEMTs with different gate geometries is extracted with an impedance analyzer, which is commonly available in any standard radio frequency testing laboratory. The main advantage is the much higher impedance coverage (from ~1 mΩ to ~100 MΩ) than other methods based on network analysis (e.g., the AC conductance method, for which accuracy is reduced by the mismatch between the AC output resistance of the device at high frequencies and the nominal resistance, typically 50 Ω, at the input ports of the vector network analyzer [12]). In contrast, a lower frequency range is achieved but still high enough to deal with electrothermal characterization.

In GaN-based HEMTs, the dependence of the thermal resistance on gate geometry has already been modeled for circuit-design purposes [12]–[16]. As far as we know, this is not the case for the thermal capacitance. To model the thermal impedance of GaN-based HEMTs, high-order *RC* thermal networks are commonly used [9], [15]–[19]. In this paper, the gate-geometry dependence of the constituting cells' components is considered and an alternative compact model is proposed, to be used in AC circuit-design.

Thus, the GaN depletion mode HEMTs (D-HEMTs) considered here, with different gate widths and gate lengths, are described in Section II. The experimental setups used for characterization and validation of the thermal impedance are described in Sections III and IV, respectively. Section V is devoted to the thermal impedance characterization, results,

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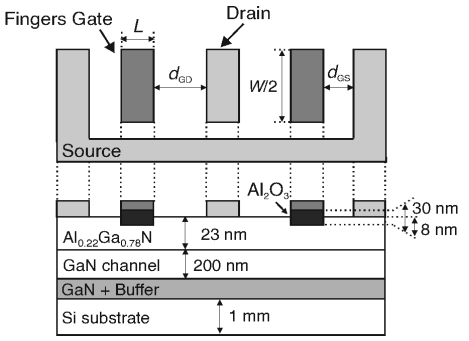


Fig. 1. Top and cross-sectional views of the device structure under study (drawing not to scale).

and modeling. Finally, the conclusions are discussed in Section VI.

## II. Fabricated Devices

The AlGaN/GaN layer stack of the D-HEMTs investigated here (provided by CEA-Leti) consisted of Ga(Al)N epitaxial layers grown on a 1 mm thick Si substrate in the (1-1-1) direction [20], with a non-intentionally doped GaN channel and $Al_{0.22}Ga_{0.78}N$ barrier, which were 200 and 23 nm thick, respectively. The transistors were based on a partial $Al_{0.22}Ga_{0.78}N$ etching, with a gate recess of 8 nm, to give a negative threshold voltage of −4 V, using a TiN/W (double finger) gate metal and $Al_2O_3$ gate oxide, of 30 nm thickness.

A reference device with a gate length, $L$, of $L_{ref}$ = 2 µm and a gate width, $W$, of $W_{ref}$ = 100 µm (2 × 50 µm) was characterized. Devices with other gate lengths (3 and 4 µm) and total widths (40 and 200 µm) were also measured. In all cases, the gate-to-source separation, $d_{GS}$, and gate-to-drain extension, $d_{GD}$, were 2 and 15 µm, respectively. The top and cross-sectional views of the device structure under study are shown in Fig. 1, where the main dimensions are labeled.

## III. Experimental Setup

On-wafer measurements were performed with a Cascade Summit 9000 probe station. The measurement setup, which stands out in its simplicity, is described in Fig. 2(a). By using the auto-balancing bridge method [11], $Y$ parameters were measured at room temperature (25 °C) from 20 Hz to 10 MHz with an impedance analyzer (Keysight E4990A), a port extension cable (16048H), and a Cascade signal-ground-signal microprobe contacting the source-gate-drain terminals. To calibrate the measurement system, a 100 Ω load resistor (E4990-61001), furnished with an impedance analyzer, was employed. At the frequency range used, the influence of the probe and the pad parasitics is negligible.

The longitudinal electrical field, in the channel of the devices, was limited to low levels, to avoid the activation of trap states and, therefore, a misshaped output admittance frequency response but, at the same time, high enough for the power dissipation to change the channel temperature [6]. Thus, the quiescent condition was 5 V for the drain-source voltage, $V_{DQ}$, via the internal bias tee of the impedance analyzer, with the gate terminal being grounded through the

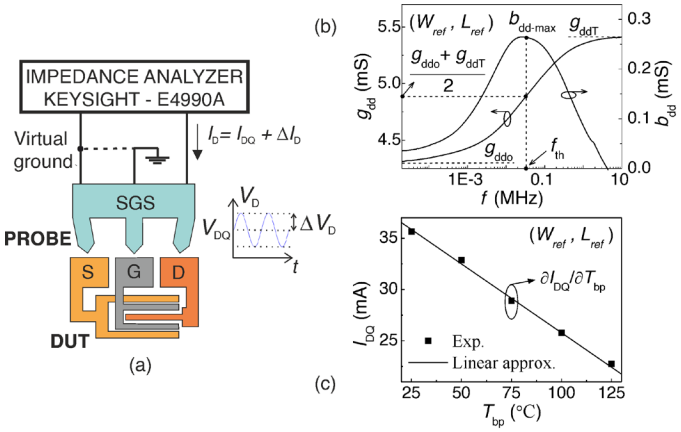


Fig. 2. Schematic of the experimental setup (a); AC parameters (b) and DC parameters (c) of interest for the reference device with $V_{DQ}$ = 5 V.

common microprobe tip for a null gate-source voltage; $V_{GQ}$ = 0 V. This last restriction does not invalidate the electrothermal technique used here, since thermal characteristics of the D-HEMTs can be determined by $V_{DQ}$.

To obtain the temperature dependence of the quiescent drain current, $I_{DQ}$, the bare dies were placed directly on a hotplate to maintain the base-plate temperature, $T_{bp}$, in the range 25−125 °C, at increments of 25 °C. Thus, a negative $I_{DQ}$-$T_{bp}$ linear coefficient was extracted (no trapping-induced positive $I_{DQ}$-$T_{bp}$ coefficient was observed [6]).

## IV. Validation Setup

In order to validate the frequency domain characterization, the thermal resistance of the HEMTs was also obtained with the pulsed method shown in Fig. 3(a). In this case, the drain current ($I_D$) was determined based on Ohm's law, with the drain terminal being pulsed through a 50 Ω sensing resistor. The voltage drop [see Fig. 3(a)], $\Delta V_{DD} = V_{DD} - V_D$, was measured with an Agilent DSO6032A oscilloscope. By making use of an Agilent B1500A semiconductor analyzer for biasing and a Cascade ground-signal-signal microprobe contacting the source-gate-drain terminals, pulsed output characteristics were measured by varying the base-plate temperature for $V_{GQ}$ = 0 V. The devices were excited with

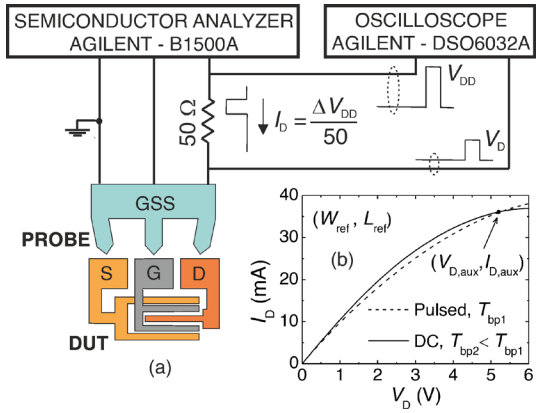


Fig. 3. (a) Schematic showing the setup used for validation; (b) DC and pulsed parameters of interest for the reference device with $V_{GQ}$ = 0 V, $T_{bp1}$ = 25 °C, and $T_{bp2}$ = 50 °C.

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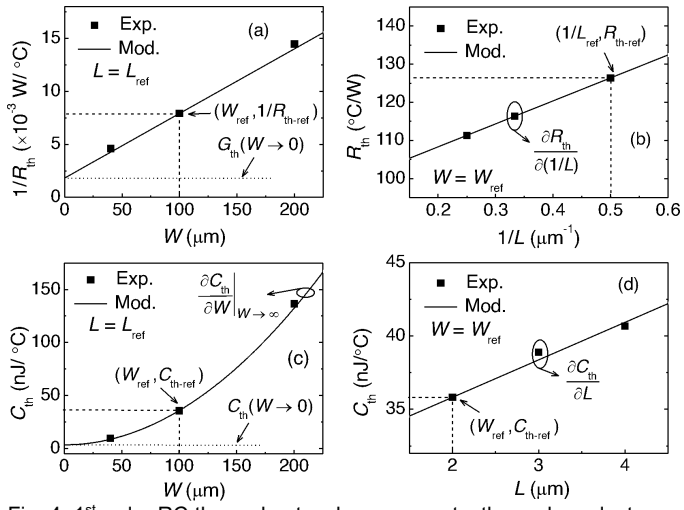


Fig. 4. 1st order RC thermal network components: thermal conductance ($1/R_{th}$) with gate width for $L = L_{ref}$ (a); thermal resistance with $1/L$ for $W = W_{ref}$ (b); thermal capacitance with gate width for $L = L_{ref}$ (c); thermal capacitance with gate length for $W = W_{ref}$ (d). Measured and modeled data are shown with symbols and lines, respectively.

TABLE I
AC MODEL PARAMETERS

| | | | | | |
|---|---|---|---|---|---|
| $a$ (μm) | 29.7 | $L_1$ (μm) | 0.4 | $W_{ref}$ (μm) | 100.0 |
| $b$ ($\times 10^{-5}$ μm$^{-1}$) | 4.4 | $L_2$ (μm) | 14.0 | $R_{th-ref}$ (°C/W) | 126.4 |
| $c$ ($\times 10^{-4}$ μm$^{-2}$) | 9.4 | $L_{ref}$ (μm) | 2.0 | $C_{th-ref}$ ($\times 10^{-9}$ J/°C) | 35.8 |

positive short-pulsed drain voltages of duration 200 ns, from a zero power dissipation quiescent bias point ($V_{DQ}$ = 0 V), with a duty cycle of 0.02% to avoid self-heating effects [4].

## V. THERMAL IMPEDANCE CHARACTERIZATION AND MODELING

### A. Characterization

According to the frequency domain characterization [21], the output conductance, $g_{dd}$, and the output susceptance, $b_{dd}$, can be approximated by (1) and (2):

$$g_{dd} \approx g_{ddT} + \mathrm{Re}(Z_{th}) \cdot \frac{\partial I_{DQ}}{\partial T} \cdot \left( V_{DQ}\, g_{ddT} + I_{DQ} \right), \tag{1}$$

$$b_{dd} \approx \omega C_{ddT} + \mathrm{Im}(Z_{th}) \cdot \frac{\partial I_{DQ}}{\partial T} \cdot \left( V_{DQ}\, g_{ddT} + I_{DQ} \right), \tag{2}$$

where $g_{ddT}$ and $C_{ddT}$ are the output conductance and output capacitance at high frequency, respectively (with dynamic self-heating removed). $Z_{th}$ represents the thermal impedance of the device and $\omega$ is the angular frequency, $2\pi f$.

The lines in Fig. 2(b) represent the measured output conductance (left axis) and output susceptance (right axis) frequency response for the reference device. It should be noted that a maximum output susceptance is obtained at the characteristic thermal frequency, i.e., $b_{dd,max} = b_{dd}(f_{th})$ with $\omega_{th} = 2\pi f_{th} = 1/\tau_{th}$, when $g_{dd}(f_{th}) = (g_{ddT} + g_{ddo})/2$ [22], [23]. Similar results were obtained for the rest of the devices.

No dependence of $f_{th}$ on $L$ was observed. However, $f_{th}$ diminishes as $W$ increases (not shown).

All of the required frequency domain parameters and the quiescent drain current for the extraction of the thermal impedance are provided by the impedance analyzer. By varying the base-plate temperature, a linear temperature dependence of $I_{DQ}$ resulted, as Fig. 2(c) shows for the reference device, from which $\partial I_{DQ}/\partial T_{bp}$ was determined.

In the case of the pulsed technique, the output characteristics for the reference device at a base-plate temperature of $T_{bp1}$ = 50 °C and $V_{GQ}$ = 0 V are shown in Fig. 3(b) as a dashed line. It should be noted that the same DC current $I_{D,aux}$ is obtained at a lower base-plate temperature $T_{bp2}$ = 25 °C for $V_{D,aux}$. From this point, ($V_{D,aux}$, $I_{D,aux}$), the thermal resistance is $R_{th} = \Delta T_{bp}/P_{aux}$, where $\Delta T_{bp}$ is the difference between the corresponding substrate temperatures for the pulsed and DC measurements, $T_{bp1} - T_{bp2}$, and $P_{aux} = I_{D,aux} V_{D,aux}$ is the power dissipation.

### B. AC Compact Model

By using a first-order thermal network, i.e., with $1/Z_{th} = 1/R_{th} + j\omega C_{th}$, the thermal resistance of the device $R_{th}$ is obtained from (1) as follows:

$$R_{th} = \frac{g_{ddo} - g_{ddT}}{\dfrac{\partial I_{DQ}}{\partial T_{sub}} \times \left( V_{DQ} g_{ddT} + I_{DQ} \right)}, \tag{3}$$

where $g_{ddo} = g_{dd}(\omega \to 0)$ is the output conductance at low frequency and $C_{th}$ is the thermal capacitance of the device. In this case, it can be easily demonstrated that the maximum output susceptance is obtained at the characteristic thermal frequency ($\partial b_{dd}/\partial\omega = 0$ at $\omega = \omega_{th}$), where $g_{dd}(f_{th}) = (g_{ddT} + g_{ddo})/2$ and $C_{th} = \tau_{th}/R_{th}$ [22], [23].

The expected gate-geometry dependence of the thermal resistance (3), with $R_{th}$ decreasing when both gate width and gate length expand because more heat flow can be spread out of the device through the terminals, can be modeled as:

$$R_{th} = R_{th\text{-}ref} \cdot \frac{W_{ref} + a}{W + a} \cdot \left[ 1 + L_1 \left( \frac{1}{L} - \frac{1}{L_{ref}} \right) \right], \tag{4}$$

with fitting parameters $a$ (indicating that heat dissipation from hot channel region is not just parallel to current flow and vertical through the substrate and terminals, but also transverse via the gate metal or the substrate [24]) and $L_1$, which are shown in Table I together with the thermal resistance of the reference device, $R_{th\text{-}ref}$. The modeled values of thermal conductance, $G_{th} = 1/R_{th}$, and thermal resistance (with $W$ and $1/L$, respectively) are indicated by lines in Figs. 4(a) and (b), and extracted data are shown by symbols.

Similar values for the normalized thermal resistance (°C-mm/W) of GaN-on-Si HEMTs were obtained in [8], [12]–[14]. In addition, good agreement was observed between the thermal resistances obtained by the frequency domain and pulsed techniques, with values of 126.4 and 129.9 °C/W for the reference device, respectively (similar agreement was obtained for the rest of the devices).

By knowing the characteristic thermal frequency of the D-HEMTs, the gate width and gate length dependence of the thermal capacitance, $C_{th}$, was obtained as $\tau_{th}/R_{th}$ [22], [23] and represented by symbols in Figs. 4(c) and (d), respectively. The

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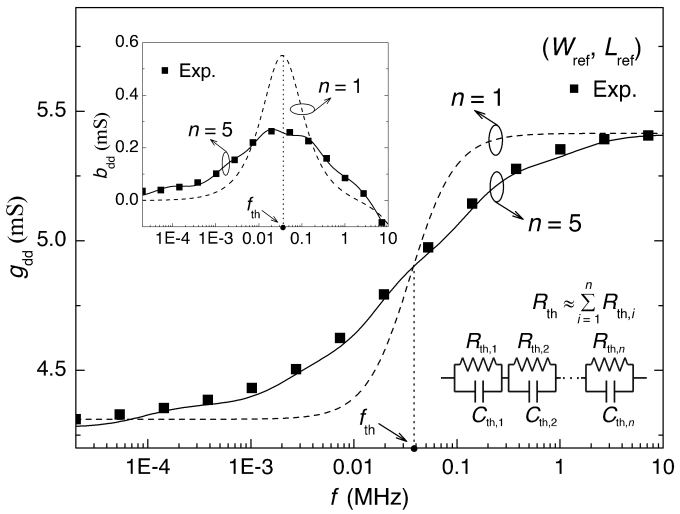


Fig. 5. Output conductance frequency response: measured data (symbols) and modeled data by means of one and five thermal time constants (dashed and solid line, respectively). Analogously, the inset shows the output susceptance frequency response.

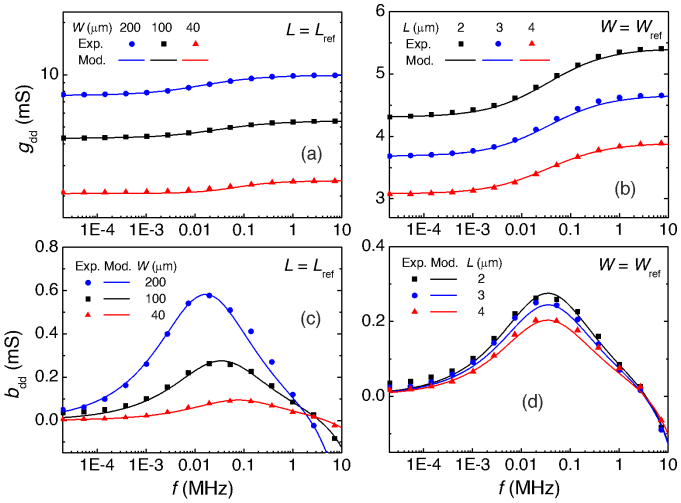


Fig. 6. AC compact model: measurements (symbols) and modeled data with the novel approach (lines) of the conductance frequency response for different gate widths where $L = L_{ref}$ (a), different channel lengths with $W = W_{ref}$ (b), and the corresponding susceptance frequency response, (c) and (d), respectively.

corresponding thermal time constants range from 1-10 μs, which is consistent with those obtained in [25]–[27] for GaN-on-Si HEMTs.

It should be noted that a linear gate width dependence of the thermal capacitance is obtained for sufficiently large gate widths, when transversal thermal effects are negligible. In addition, as expected from [28], the thermal capacitance is proportional to the gate length. Thus, the modeled thermal capacitance, indicated by a line in Figs. 4(c) and (d), can be expressed as follows:

$$C_{th} = C_{th\text{-}ref} \cdot \frac{1+bW_{ref}}{1+bW} \cdot \frac{1+cW^2}{1+cW_{ref}^2} \cdot \left(1 + \frac{L - L_{ref}}{L_2}\right), \quad (5)$$

where $b$, $c$, and $L_2$ are fitting parameters, which are shown in Table I together with the thermal capacitance of the reference device, $C_{th\text{-}ref}$.

From (4) and (5), we obtain the thermal impedance $Z_{th\text{-first order}}$ as

$$Z_{th\text{-first order}} = \frac{R_{th}}{1+(\omega\tau_{th})^2} - j\,R_{th} \cdot \frac{\omega\tau_{th}}{1+(\omega\tau_{th})^2}, \quad (6)$$

where $\tau_{th} = R_{th}C_{th}$. In this case, as shown in Fig. 5 for the reference device, where the measured and modeled output conductance frequency response is represented by symbols and a dashed line, respectively, $g_{dd}$ is undervalued/overvalued at frequencies lower/higher than $f_{th}$. Correspondingly, the inset shows the output susceptance frequency response, where $b_{dd}$ is overvalued at frequencies near to $f_{th}$, and undervalued at frequencies far from it.

To adequately reproduce the output conductance and output susceptance frequency response, we use a simple, design-oriented method that consists of replacing $(\omega\tau_{th})$ by $(\omega\tau_{th})^{0.35}$ and $(\omega\tau_{th})^{0.5}$ in the real and imaginary parts of $Z_{th\text{-first order}}$, respectively, with a minimum thermal reactance of $-R_{th}/4$ (half of the initial prediction). The AC thermal impedance, $Z_{th\text{-AC}}$, can be approximated as

$$Z_{th\text{-AC}} \approx \frac{R_{th}}{1+(\omega\tau_{th})^{0.7}} - j\,\frac{R_{th}}{2} \cdot \frac{(\omega\tau_{th})^{0.5}}{1+\omega\tau_{th}}. \quad (7)$$

Under these assumptions, the maximum output susceptance still takes place at the characteristic thermal frequency, i.e., $b_{dd,max} = b_{dd}(f_{th})$, when $g_{dd}(f_{th}) = (g_{ddT} + g_{ddo})/2$. The resulting modeled output conductance (1) and output susceptance (2) for the D-HEMTs, where $Z_{th} = Z_{th\text{-AC}}$, are represented in Fig. 6 by lines, in excellent correspondence with the measured data represented by symbols and demonstrating the validity of (7) for any gate geometry.

This knowledge can be used for the identification of a gate geometry-dependent electrothermal model for GaN-based HEMTs, to be used in AC circuit-design, when simplification is mandatory when dealing with compact models.

### C. *Gate Geometry-Dependent Thermal Network*

To accurately reproduce the heating dynamics in the time domain, the devices were described from a thermal point of view by means of a fifth-order *RC* Foster thermal network, at the expense of a higher computational cost [9], [29]. The thermal resistance, $R_{th,i}$, and thermal capacitance, $C_{th,i}$, of each cell $i$ ($i$ = 1, 2, 3, 4, 5) were extracted by fitting the imaginary part of the output susceptance (2) for closer results [30], using the least-squares method and initial values of $R_{th}/5$ and $5C_{th}$, respectively, where $R_{th}$ and $C_{th}$ are given by (4) and (5), respectively. The modeled results for $g_{dd}$ (1) and $b_{dd}$ (2) for the reference device are shown in Fig. 5 as solid lines, and these correspond well with the measured data.

This being so, the sum of the resulting resistive components keeps close to $R_{th}$ (129.8 ≈ 126.4 °C/W for the reference device), as in [30], which is not the case with the reciprocal of the corresponding capacitances. This could be attributed to the capacitors of the Foster thermal network not being connected to the ground. In a Foster thermal network, each internal node is crossed by the current coming from the preceding resistance and from the back side of the preceding capacitor, which has

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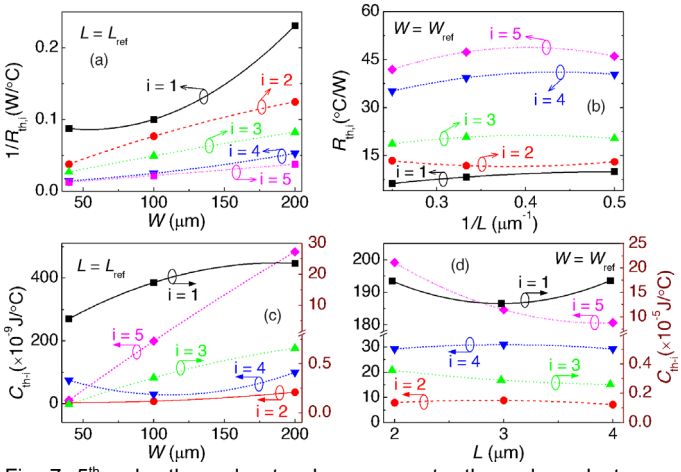


Fig. 7. 5th order thermal network components: thermal conductances ($1/R_{th,i}$) with gate width for $L = L_{ref}$ (a); thermal resistances with $1/L$ for $W = W_{ref}$ (b); thermal capacitances with gate width for $L = L_{ref}$ (c); thermal capacitances with gate length for $W = W_{ref}$ (d). Extracted and modeled data are shown with symbols and lines, respectively.

TABLE II
FOSTER THERMAL NETWORK PARAMETERS

| $i$ | 1 | 2 | 3 | 4 | 5 |
|---|---|---|---|---|---|
| $R_{th\text{-}ref,i}$ (°C/W) | 10.0 | 13.1 | 20.4 | 40.4 | 46.1 |
| $C_{th\text{-}ref,i}$ (× $10^{-8}$ J/°C) | 17325.2 | 0.8 | 356.8 | 2.9 | 19.9 |
| $a_{i1}$ (× $10^{-4}$ W /°C-μm) | 6.2 | 5.9 | 3.6 | 2.2 | 1.6 |
| $a_{i2}$ (× $10^{-7}$ W /°C-μm$^2$) | 68.6 | −10.7 | −2.9 | 6.5 | 0.4 |
| $b_{i1}$ (°C-μm/W) | 1.2 | 24.6 | −20.5 | −22.2 | −56.7 |
| $b_{i2}$ (°C-μm$^2$/W) | −54.7 | 103.8 | −109.2 | −172.4 | −292.9 |
| $c_{i1}$ (× $10^{-9}$ J/°C-μm) | 1454.1 | 0.2 | 39. 8 | −0.2 | 3.0 |
| $c_{i2}$ (× $10^{-11}$ J/°C-μm$^2$) | −829.6 | 0.1 | −9.4 | 0.9 | −0.2 |
| $d_{i1}$ (× $10^{-8}$ J/°C-μm) | −9277.1 | 0.2 | −86.8 | 0.3 | −2.0 |
| $d_{i2}$ (× $10^{-8}$ J/°C-μm$^2$) | 4659.3 | −0.1 | 19.3 | −0.2 | 0.5 |

no physical meaning from a thermal point of view (there are no quantities corresponding to the negative electric charge in thermal circuits) [29].

Fig. 7 shows the gate geometry dependence of the extracted resistive and capacitive components (with symbols), which must be accurately reproduced to avoid a misshaped output admittance frequency response. Thus, by using second-order polynomials as table lookup models, $R_{th,i}$ and $C_{th,i}$ are given by (8) and (9):

$$R_{th,i} = \frac{R_{th\text{-}ref,i} + \sum_{j=1}^{2} b_{ij}\left(\frac{1}{L} - \frac{1}{L_{ref}}\right)^{j}}{1 + R_{th\text{-}ref,i}\sum_{j=1}^{2} a_{ij}(W - W_{ref})^{j}}, \tag{8}$$

$$C_{th,i} = \frac{C_{th\text{-}ref,i} + \sum_{j=1}^{2} c_{ij}(W - W_{ref})^{j}}{\left[1 + \frac{\sum_{j=1}^{2} d_{ij}(L - L_{ref})^{j}}{C_{th\text{-}ref,i}}\right]^{-1}}, \tag{9}$$

which are represented by lines in Fig. 7, with fitting parameters $a_{ij}$ , $b_{ij}$, $c_{ij}$ , $d_{ij}$, and the $R_{th\text{-}ref,i}$ and $C_{th\text{-}ref,i}$ of the reference device, being particularized for each cell and shown in Table II. The gate geometry-dependent modeled $g_{dd}$ (1) and $b_{dd}$ (2) are in good correspondence with the measured data, as Fig. 8 shows with lines and symbols, respectively.

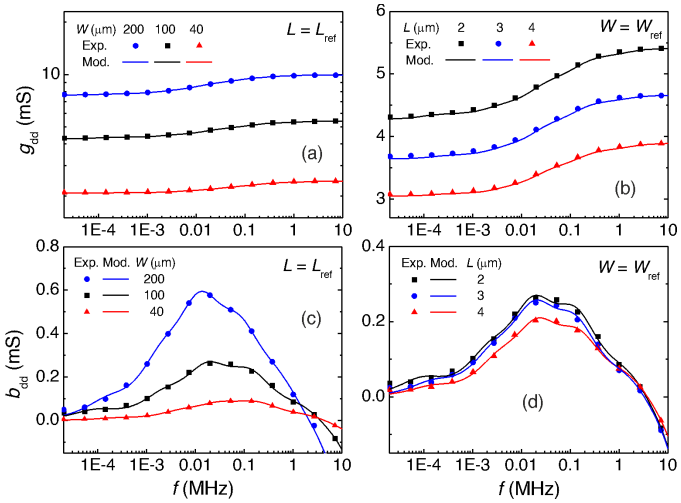


Fig. 8. Measurements (symbols) and modeled data with the 5th order thermal network (lines) of the conductance frequency response for different gate widths where $L = L_{ref}$ (a), different channel lengths with $W = W_{ref}$ (b), and the corresponding susceptance frequency response, (c) and (d), respectively.

## VI. CONCLUSIONS

The thermal impedance of GaN D-HEMTs on silicon has been successfully measured using frequency domain characterization. The dependence of the thermal impedance on gate geometry was observed and modeled for circuit-design purposes. A first-order *RC* thermal network adjusted in frequency response is sufficient for the admittance frequency response to be correctly reproduced. For a time domain analysis, the dependence on the gate geometry of the cell components constituting a fifth-order RC Foster thermal network was obtained. The modeling approaches presented to account for self-heating effects and varying the gate geometry, can be easily incorporated in circuit simulators as an add-onto other well established models.

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