Capacitance Characterization of Coupled Transmission Lines Applied to VLSI Interconnections Modelling

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Abstract

The calculation of the electrical parameters of transmission lines inside CMOS integrated circuits is presented. It is shown that a commonly used 2-D device simulator, MEDICI, can be employed to compute the electrical parameters. In particular, decreasing size dimensions in interconnections makes parasitic coupling capacitance more important. In this work we propose a set of design rules to reduce the coupling problem in the future developments in VLSI interconnection and their impact on peak crosstalk in 0.18 μm. In order to estimate crosstalk noise in the signal lines, SPICE simulations have been used.

Introduction

In modern high-speed VLSI chips and multichip modules, interconnects are playing an increasingly important role. In designing a reliable system, a model for distributed transmission line is necessary in order that the interconnection effects can be analysed [1]. To achieve a higher level of integration, the cross-sectional dimensions of the interconnections have to be scaled down. This implies two things: first, the resistance per unit length of the lines increase and the effect must be taken into account in the transmission modelling. Second, the parasitic coupling capacitance increases also because of smaller distance between interconnections. This parasitic coupling produces spurious signals that, under certain conditions like high switching speed and mixing of devices with different driving capabilities, may be important enough to affect logically the circuit [2]. To optimize the functional performance of high-speed printed circuits and similar microwave and millimeter-wave integrated circuits, the inclusion of crosstalk analysis is very important to determine the overall functional performance of the circuits. Because modelling and simulation are practical necessities for modern design, it is important that the models representing the system to be accurate enough to reproduce the voltages, currents and waveforms in simulation to an acceptable error tolerance.

The central problem in the computation of the distributed parameter transmission line is the solution of the Laplace equation in two dimensions subject to appropriate boundary conditions. There are many approaches to solve this equation, in this work we based on the MEDICI simulator (involving a Finite element Method), a 2-D device

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simulator used extensively in the semiconductor industry to calculate the electrical parameters of 2-D structures by an ac-small signal analysis from the electric field distribution [3, 4, 5].

This work provides a set of design rules to minimize the coupling problem in the future developments in VLSI interconnection and their impact on peak crosstalk in 0.18 μm. To do this, a typical one and two levels coupled lines configuration on different p-type substrates with high and low resistivity has been studied. The self and mutual capacitances in the scaled-down VLSI's are also introduced. In addition we prove how the differences in material and device parameters affect the performance of the result. To estimate crosstalk noise in the signal lines SPICE simulations have been used [6, 7].

Structures Under Study

With the rapid evolution of VLSI technology, minimum feature size and the distance between interconnections continue to decrease. Thus, transmission line effects such as crosstalk will play an important role in determining system performance. Crosstalk effects in voltage response are due to mutual capacitances and inductances between adjacent lines. The coupling between lines increases as separation between the lines decreases, as the distance to the ground plane increases, and as the distance over which the line neighbour each other increases. In addition, crosstalk effects increase as characteristic impedance (Z_0) increases since capacitance of the line to the ground plane and the coupling capacitance will have greater effect on the signal voltage [8]. In many standard books and papers several methods have been discussed in detail to deal with the electrical parameters. Two dimensional device simulation using MEDICI was carried out to characterize the performance of the structures under study with different configurations and dimensions (numerical methods accurately calculate interconnect electrical parameters using finite element methods [3, 9]). This simulator allows the extraction of the capacitance matrix per unit lentgh between all the element defined in the device by an ac-small signal analysis from the electric field distribution. In this work, two types of configurations have been studied: single layer and two-layer coupling of width **w** height **t** and separation **s**, embedded in a SiO_2 dielectric layer as shown in fig. 1. The conductors in the mentioned stuctures are modeled by a heavily doped semiconductor [10]. The lines are suspended at an altitude **h** over the p-type substrate.

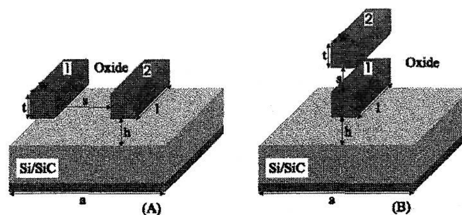

Figure 1: The cross section of the conductors for the structures analyzed

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Capacitances of the Coupled Interconnect Systems

An interconnection can be described by means of the electrical parameters: resistance, capacitance and inductance. The values of these parameters depend on the physical description (geometry and material) of the structure. However, not all the parameters are necessary when computing the response of the line at the transmission of an electrical signal. Then, in this paper the interconection are modelled as a lumped capacitance. The simulation results presented in this paper are computed based on the

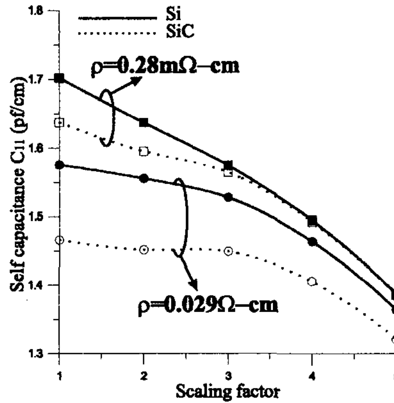

Figure 2: Self capacitance evolution with scaling down for fig 1. (A)

capacitances matrix determined by MEDICI [4]. The evolution of these capacitances have been studied with geometric scaling down. To compare the influence of the distinct materials with different concentration, we present some figures to show that for a given low values of scaling down, coupling increases but also depends on the substrate material characteristics.

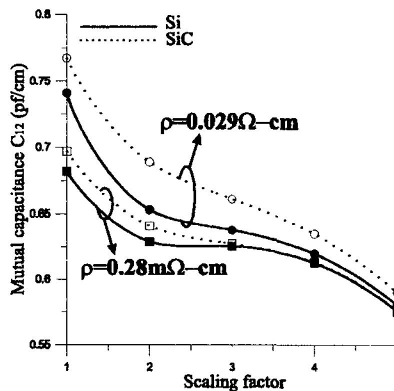

Figure 3: Mutual capacitance evolution with scaling down for fig 1. (A)

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Capacitance dependence is obtained by comparing the effect of the two materials with high and low resistivity which are summarized in Figures 2 and 3 corresponding to the case (A): single layer structure. It is shown that for a low values of scaling down the difference between the results increases too much, this means that big reduction can be noted when the crosstalk voltage is measured, as seen in the next section. As depicted in the previous figures, both the self and the mutual capacitance increase as the dimensions of the configuration decreases.

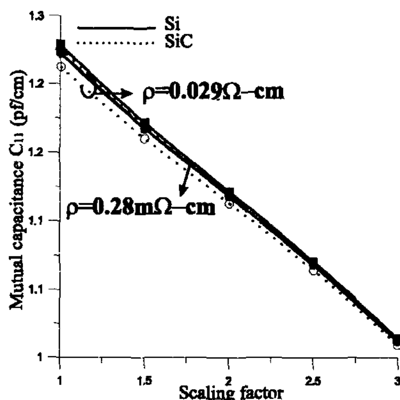

Figure 4: Self capacitance evolution with scaling down for fig 1. (B)

It is interesting to note, how much these capacitances per unit length of the line are affected when the substrate (Si or SiC) is highly doped and the structure dimensions is very small. It is clear that the decreasing dimensions geometries and highly doped substrate can help us to reduce the coupling effects, precisely when the SiC substrates are used.

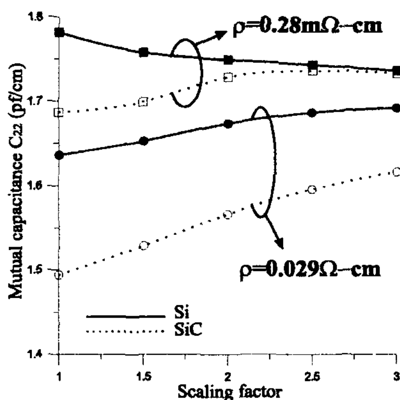

Figure 5: Self capacitance evolution with scaling down for fig 1. (B)

As noted above, the decreasing cross-sectional dimensions in interconnections cause an

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increase in line capacitance, we also represent in the figures 4, 5 and 6 for the double layer structure fig. 1 (B), the evolution of the self and mutual capacitances with the scaling down. It can be seen from the results obtained that the same observations done before (fig. 2 and 3) can be applied for both capacitances.

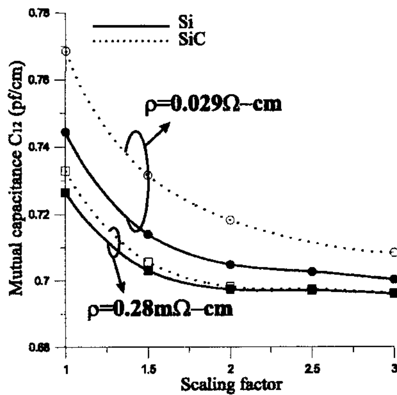

Figure 6: Mutual capacitance evolution with scaling down for fig 1. (B)

Crosstalk Analysis

Since the determination of a capacitance matrix per unit lentgh between all the elements defined in the devices has been performed, we will next study the coupling noise dependence on important physical parameters of the lines. The interference noise between the adjacent lines 1 and 2 is considered as the superposition of a capacitive coupling. *The lines configuration are the same as shown in the Fig. 1 and its equivalent* model circuit is presented in the fig. 7. Traditionally, SPICE simulations have been used to estimate crosstalk noise in the signal lines.

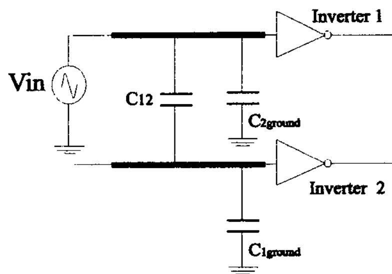

Figure 7: Crosstalk modelling equivalent circuit proposed for fig. 1

The figures 8, 9, 10 and 11 show the dependence of the crosstalk voltage on the interconnection length, resistivity of the substrates and the scaling coefficients in the range

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10 to 100 μm. In each case we have represented for the two different substrates the same curves for a high and low scaled degrees, for example fig.7 ((a): small structure size, (b): big structure size, thus for all the structures that follow). Significant improvement in the crosstalk effect can be achieved when the Si substrate with high resistivity and longer interconnect length have been used. It is observed also that the crosstalk voltage increases as the line length increases. All figures demonstrate that the crosstalk interference become important when the scaling coefficient decreases. In addition, it can be noticed how the material characteristics can cause a significant increase or a reduce of the crosstalk coupling between signals. For example, all figures illustrate the length dependences of crosstalk for the Si and SiC. It is clear that when Si substrate with high concentration is used and the value of interconnect cross-sectional dimensions becomes small, the effect of crosstalk voltage is smaller than the corresponding to SiC materials. This comparison becomes more significant when the length lines is longer.

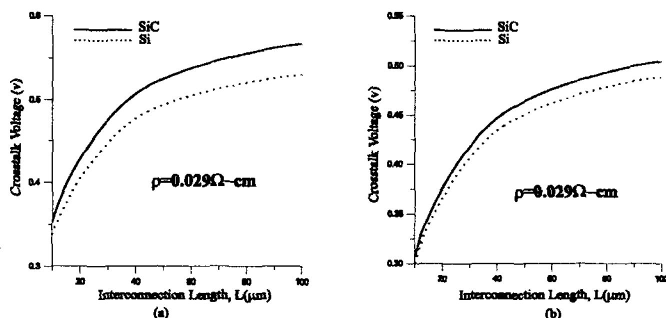

Figure 8: Dependence of the crosstalk voltage on the interconnection length for the single-level interconnections for the low and high scaling coefficients is shown in figures (a) and (b) respectively. The line system is shown in Fig. 1. (A)

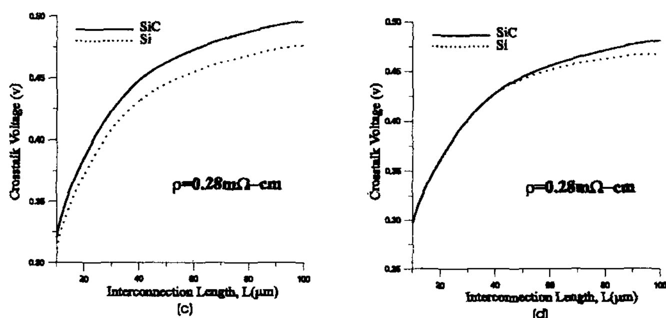

Figure 9: Dependence of the crosstalk voltage on the interconnection length for the single-level interconnections for the low and high scaling coefficients is shown in figures (c) and (d) respectively. The line system is shown in Fig. 1. (A)

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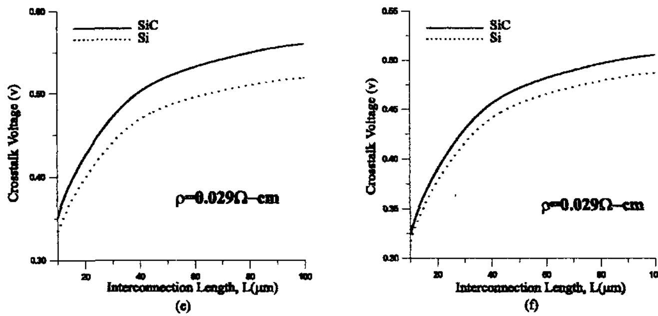

Figure 10: Dependence of the crosstalk voltage on the interconnection length for the double-level interconnections for the low and high scaling coefficients is shown in figures (e) and (f) respectively. The line system is shown in Fig. 1. (B)

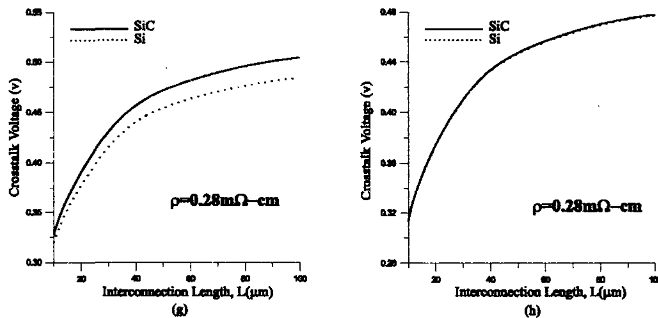

Figure 11: Dependence of the crosstalk voltage on the interconnection length for the double-level interconnections for the low and high scaling coefficients is shown in figures (g) and (h) respectively. The line system is shown in Fig. 1. (B)

Conclusions

Values for parasitic capacitances between metal lines in a 0.18 μm. technology have been obtained by means of simulation, for different cases, and evolution of these capacitances with scaling down has been studied. An equivalent circuit for crosstalk analysis has been presented, and with the capacitance data previously obtained, SPICE simulations of the circuit have been made in order to find the evolution of crosstalk voltage with different interconnection lengths, resistivity of the substrates and the scaling coefficients. It has been noticed that significant improvement in the crosstalk effect can be achieved for a high resistivity and small dimensions devices for different intecconnection length.

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