# RF Extraction of Thermal Resistance for GaN HEMTs on Silicon

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***Abstract*—In this article, an AC conductance method has been successfully employed to extract the thermal resistance of GaN-based HEMTs on silicon. The resulting thermal resistances, when varying the channel length and gate width, are comparable to those obtained with pulsed measurements, by making use of positive drain-to-source pulsed voltages from a zero power dissipation quiescent bias point, and 3-D thermal simulations. Furthermore, the gate geometry dependence of the thermal resistance of GaN-based HEMTs has been successfully modeled for circuit-design purposes.**

*Index Terms*—**Thermal resistance, electrothermal characterization, gallium nitride, high-electron mobility transistors (HEMTs), AC/pulsed measurement.**

## I. Introduction

Thermal effects can be critical in the performance of radio frequency and high-power integrated circuit applications [1]−[4]. When silicon-on-insulator (SOI) technology is used, the buried oxide layer (BOX) significantly prevents heat transfer toward the substrate [5]. With advanced semiconductor materials, such as GaN-based compound semiconductors, a significant heat generation in the channel of high-power devices can be present [6] that can even vary their asymmetric access resistances [7], [8]. In any case, characterization and modeling of the thermal resistance of transistors are essential for a proper circuit and package design.

For SOI metal-oxide-semiconductor field-effect transistors (MOSFETs), several precise techniques have been developed to measure the thermal resistance, which are mainly based on the AC conductance method [9]−[11] and pulsed characteristics [12], [13]. Similarly, for GaN-based high-electron mobility transistors (HEMTs) pulsed characteristics [14], [15] have successfully been used to extract the thermal resistance, in addition to techniques such as step response [16], IR and Raman thermographs [17], or by extraction of a traps activation energy [18]. The IR thermograph is inaccurate when measuring devices with micron or sub-micron scale feature sizes. The Raman thermograph is limited to measuring device areas where optical access is not blocked by metal contacts. A combination of these techniques (e.g. step response via micro-Raman thermometry), has also been employed [19]. Particular temperature-sensitive electrical parameters (TSEP), such as the forward voltage drop between gate and source [20], the channel on-resistance [20], [21], and the gate metal resistance [22], [23], have also been used to extract the thermal resistance of HEMTs (the thermal impedance in the case of measuring the gate resistance variation in the frequency/time domain [24]). However, their use is limited by the appearance of trapping effects (due to negatively pulsed drain current) [21] and the necessity of *ad hoc* designed thermal test structures [22]−[24]. Devices with a junction-gate structure are needed in case of [20].

On the other hand, the AC conductance method can be implemented by making use of a vector network analyzer and some proper bias tees for the frequency range under use. These elements are commonly available in any standard radio frequency testing laboratory, due to their simplicity and reduced cost compared to those others required in the setups of the rest of the methods.

The thermal resistance of a test structure implemented as a GaN resistor was extracted in [25] by making use of the AC conductance method, through *S* parameters measurement. However, to the authors´ best knowledge, this technique has not been used to extract the thermal resistance of GaN-based HEMTs, which is the main objective of this paper. For validation, the thermal resistances so derived are compared with those obtained with pulsed measurements and numerical simulations, varying the gate width and gate length of HEMTs.

The resulting dependence of the thermal resistance on gate geometry has also been modeled for circuit-design purposes. Some models for GaN-based HEMTs are based on sophisticated analytical closed-form expressions [26], [27]. However, in this case, the composition of the internal layers needs to be known, which is not common for end CAD users. Alternatively, models originally used for the dependence of the thermal resistance in SOI MOSFETs on gate geometry [28] can be adopted to model the dependence of the thermal resistance in GaN-based HEMTs, as in [29].

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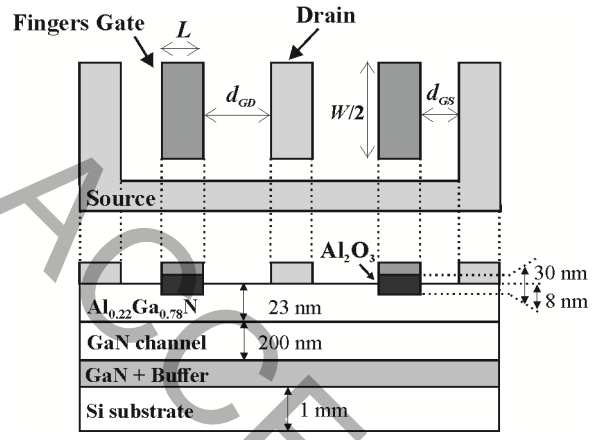



Fig. 1. Top and cross-sectional views of the device structure under study (drawings not to scale).

Thus, the GaN-based HEMTs on silicon under consideration here, with different gate widths and gate lengths, are described in Section II. The AC conductance and pulsed experimental setups used for the thermal resistance characterization are detailed in Section III. Section IV is devoted to the thermal resistance characterization, through measurements and numerical simulations, results and modeling. Finally, the conclusions are discussed in Section V.

## II. Fabricated Devices

The AlGaN/GaN layer stack of the HEMTs investigated here (provided by CEA-Leti) consisted of Ga(Al)N epitaxial layers grown on a Si substrate of thickness 1 mm in the (1-1-1) direction [30], with a non-intentionally doped GaN channel and $Al_{0.22}Ga_{0.78}N$ barrier that were 200 and 23 nm thick, respectively. The depletion-mode transistors were based on a partial $Al_{0.22}Ga_{0.78}N$ etching, with a gate recess of 8 nm, to give a negative threshold voltage of $V_{th} = -4$ V, using a TiN/W (double finger) gate metal and $Al_2O_3$ gate oxide of thickness 30 nm.

A reference device with a gate length, $L$, of 2 μm and a gate width, $W$, of 100 μm (2 × 50 μm) was characterized. Devices with other gate lengths of 3 and 4 μm and total widths of 40 and 200 μm were also measured. In all cases, the gate-to-source separation, $d_{GS}$, and gate-to-drain extension, $d_{GD}$, were 2 and 15 μm, respectively. Top and cross-sectional views of the device structure under study are shown in Fig. 1, where the main dimensions are labeled.

## III. Experimental Setup

On-wafer measurements were performed with a Cascade Summit 9000 probe station. The AC measurement setup is described in Fig. 2(a). The $S$ parameters were measured at room temperature ($T$ = 25 °C) from 100 kHz to 10 MHz with an Agilent N9913A vector network analyzer and Cascade signal-signal-ground microprobes. An Agilent B1500A semiconductor analyzer was used to bias the device under test, with DC gate and drain voltages of $V_g$ = 0 V and $V_d$ = 5 V, respectively, to enhance the self-heating effects (SHEs) [29].

In order to calibrate the measurement system, the

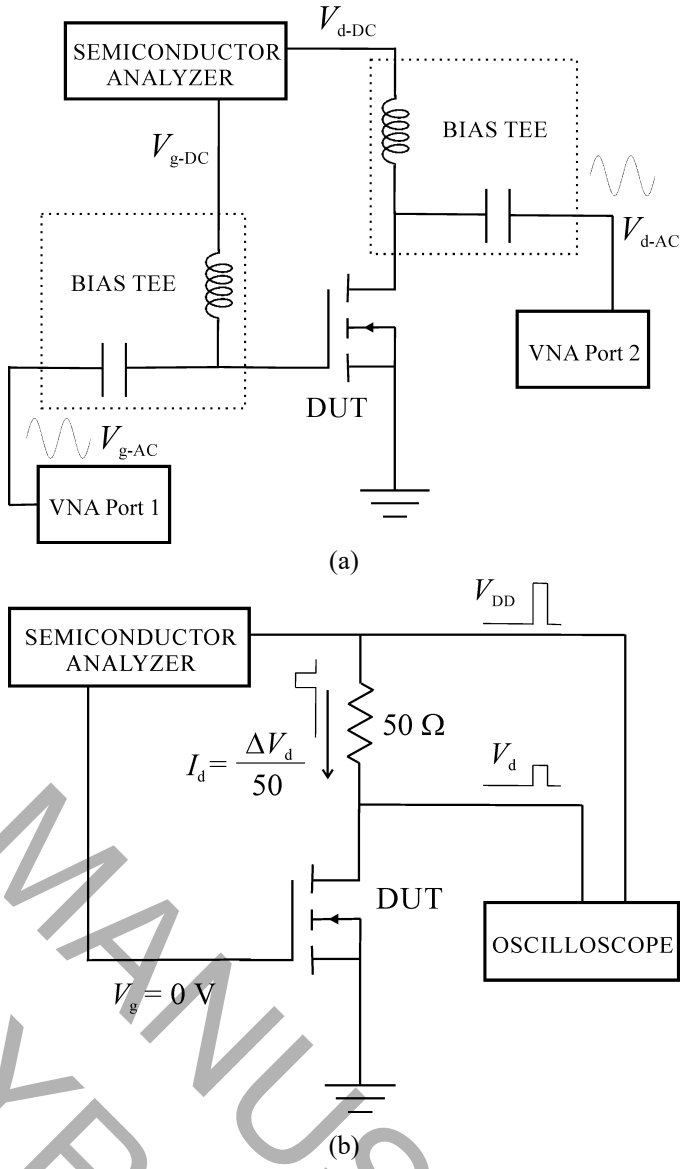



Fig. 2. (a) Schematic of an AC measurement system for the device under test and (b) experimental setup for the pulsed measurement system.

short-open-load-through method was implemented. In addition, the pad-to-device parasitic elements were eliminated with the cold-FET extraction technique that has been successfully employed in AlGaN/GaN HEMTs [7]. For that purpose, the RF access structure with an admittance matrix, $Y_{cold}$, obtained with the device in pinch-off ($V_g = -6$ V < $V_{th}$) and $V_d$ = 0 V, must be de-embedded from the measured $Y$ admittance matrix of the device at the bias point of the AC measurement setup. Then, the AC output conductance, $g_{dd}$, results the real part of $Y_{dd} - 2Y_{cold,dd} + Y_{cold,gg} - Y_{cold,gd}$ [31].

The DC parameters were measured with the Agilent B1500A semiconductor analyzer. To obtain the temperature dependence of the drain current, the transistors were placed on a hotplate. The substrate temperature was changed from 25 to 150 °C in increments of 25 °C.

In order to validate the AC conductance technique for the measurement of thermal resistance of GaN-based HEMTs, the thermal resistance was also obtained with the pulsed method

shown in Fig. 2(b). In this case, the drain current (TSEP), was determined based on Ohm's law, with the drain terminal being pulsed through a 50-Ω sensing resistor. The voltage drop was measured with the Agilent DSO6032A oscilloscope ($\Delta V_d = V_{DD} - V_d$ in Fig. 2(b)). By making use of the Agilent B1500A semiconductor analyzer for biasing, pulsed output characteristics were measured by varying the substrate temperature, for $V_g = 0$ V. The devices were excited with positive short-pulsed drain voltages of 200 ns duration, from a zero power dissipation quiescent bias point ($V_d = 0$ V), with a duty cycle of 0.02%, to avoid SHEs [15]. Thus, even with the existence of trapping phenomena, for a given drain voltage the difference between DC and pulsed drain currents was only due to SHEs. This can be attributed to the fast response of trapping phenomena, when they existed, in the order of dozens of nanoseconds [16].

## IV. Thermal Resistance Characterization and Modeling

### A. Characterization

According to the AC conductance technique [10], the output conductance frequency response is evaluated as:

$$g_{dd}(f) \approx g_{ddT} + Re(Z_{th}) \frac{\partial I_d}{\partial T} \cdot \left(V_d\, g_{ddT} + I_d\right) \quad (1)$$

where $Re(Z_{th})$ represents the real part of the thermal impedance of the device, $Z_{th}$; $g_{ddT}$ is the output conductance at high frequency (with dynamic self-heating removed); and $I_d$ is the DC drain current. Then, assuming a first-order thermal network for the thermal impedance of HEMTs, that is, $1/Z_{th} = 1/R_{th} + j\omega C_{th}$, where $R_{th}$ and $C_{th}$ are the thermal resistance and thermal capacitance of the device, respectively, the output conductance frequency response is given by:

$$g_{dd} \approx g_{ddT} + \frac{R_{th}}{1+\omega^2 R_{th}^2 C_{th}^2} \cdot \frac{\partial I_d}{\partial T} \cdot \left(V_d\, g_{ddT} + I_d\right) \quad (2)$$

Thus, in the DC regime ($\omega = 2\pi f = 0$), the following expression for the thermal resistance is derived:

$$R_{th} = \frac{g_{ddo} - g_{ddT}}{\frac{\partial I_d}{\partial T_{sub}} \cdot \left(V_d g_{ddT} + I_d\right)} \quad (3)$$

where $g_{ddo} = g_{dd}(\omega = 0) = \partial I_d / \partial V_d$ is the DC output conductance.

These parameters were obtained for all devices at the bias considered ($V_g = 0$ V and $V_d = 5$ V) in the AC experimental setup. The values of $g_{ddo}$ and $I_d$ were extracted from output characteristics at room temperature (shown with a solid line in Fig. 3 for the reference device). The output characteristics at different temperatures (shown with lines in Fig. 3 for the reference device) were used to determine the slope of the $I_d(T_{sub})$ curve at the bias considered, from the resulting linear temperature dependence of the drain current (see the inset in Fig. 3).

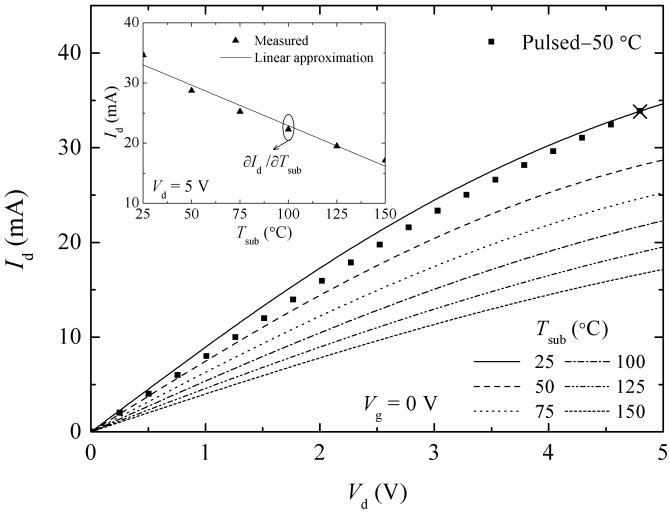



Fig. 3. Measured DC output characteristics (lines) at different substrate temperatures for the reference device and $V_g = 0$ V, and corresponding pulsed measurements at 50 °C (squares). Inset: resulting linear temperature dependence of the DC drain current for $V_d = 5$ V.

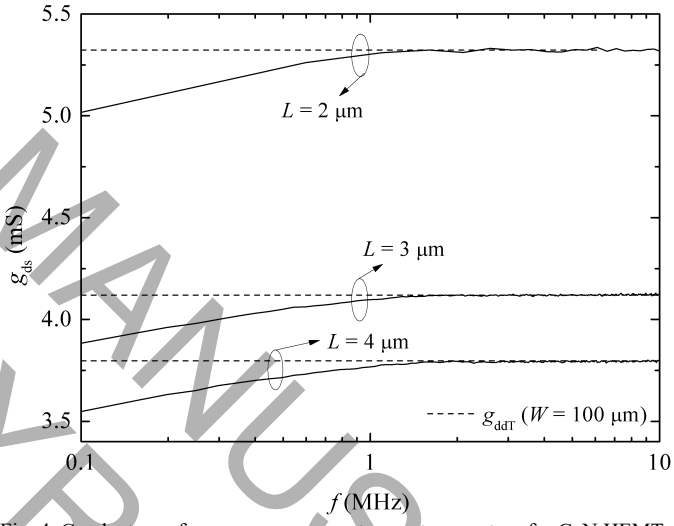



Fig. 4. Conductance frequency response at room temperature for GaN HEMTs with different gate lengths of 2, 3, and 4 μm for $V_g = 0$ V and $V_d = 5$ V.

Finally, the conductance without dynamic self-heating was extracted from the conductance frequency response (from the $S$ parameters [10]), $g_{dd}(f)$, at room temperature (solid lines in Fig. 4 for different gate lengths). Note that the conductance plateaus (i.e. when $g_{dd} \approx g_{ddT}$, with dashed lines) above 2 MHz for all gate lengths. A similar behavior has been found when varying the gate width (not shown). The measured thermal resistance of the reference device was 137 °C/W with the AC conductance technique.

In the case of the pulsed technique, output characteristics for the reference device at 50 °C and $V_g = 0$ V are shown in Fig. 3 with square symbols. It should be noted that the same DC current, $I_d = 33.74$ mA, is obtained at room temperature for $V_d = 4.81$ V, which is indicated in the figure with a cross symbol. From this point, the thermal resistance results $R_{th} = \Delta T_{sub}/P \approx 154$ °C/W, where $\Delta T_{sub} = 50 - 25 = 25$ °C is the difference between the corresponding substrate

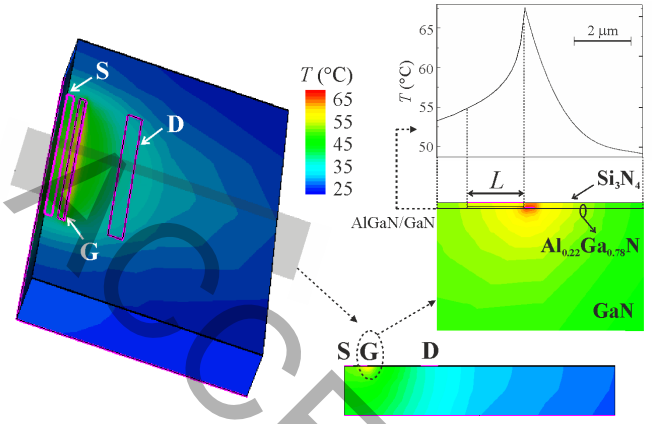



Fig. 5. Simulated temperature profile for the reference device and corresponding cross-sectional view through the gate, together with the temperature distribution at the barrier/channel heterojunction. $Q = 2$ W/mm.

temperatures for pulsed and DC measurements, and $P = I_d V_d \approx 162$ mW is the power dissipation.

A variable agreement for the thermal resistance with both AC conductance and pulsed techniques was observed for the rest of the devices, as explained in Subsection IV-B in detail. On average, only a 13% higher value for the thermal resistance with the pulsed technique is derived. Similar results were also obtained for GaN-based HEMTs on silicon in [17], [26], [27].

In addition, it must be pointed out that measurement techniques based on electrical characterization average the temperature in the active channel area. Thus, the thermal resistance of HEMTs extracted with both AC conductance and pulsed techniques predicts a device temperature lower than the peak value (located at the border of the gate by the drain side), but this is necessary for compact modeling, where average temperatures are considered.

In order to validate the gate geometry dependence of the thermal resistance that was observed with the measurement techniques, 3-D thermal simulations that included the temperature dependent thermal conductivities of the involved materials were performed with Sentaurus Device [32]. Due to the symmetry of the device, only half of it was simulated.

As in [29], where 2-D electro-thermal simulations were performed for the transistors when varying the gate-to-drain extension, Dirichlet boundary conditions for the lattice temperature (25 °C) and proper surface thermal resistances (0.009 °C-cm$^2$/W) were used at all terminals. Furthermore, the substrate was replaced by an additional equivalent surface thermal resistance (0.006 °C-cm$^2$/W). All other boundaries were assumed to be adiabatic and, for simplicity, field-plates were not considered [23].

According to [33], for transistors without field plates, or with field plates but operated at low source-drain voltages, self-heating was simulated considering a heat flux boundary condition in the channel. It consists of a 0.4 μm-long surface area of heat source at the barrier/channel heterojunction, adjacent to the drain edge of the gate contact, where a uniform power dissipation density, $Q$, of 2 W/mm was assumed.

Consistent with the fact that our measurement techniques

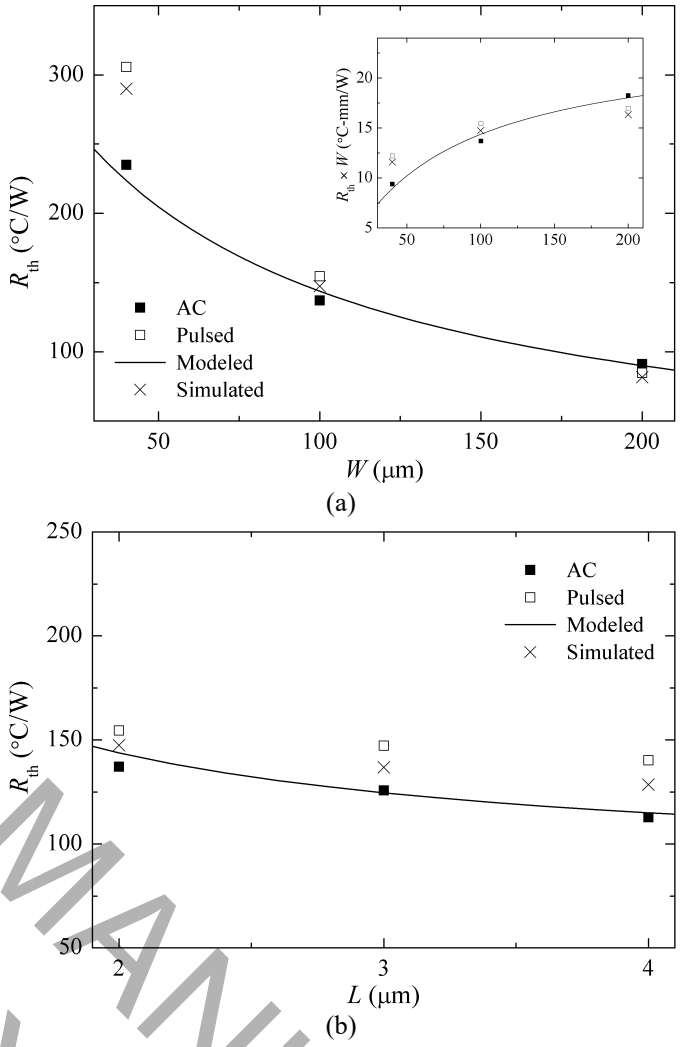



Fig. 6. Thermal resistance with (a) gate width for $L = 2$ μm and (b) channel length for $W = 100$ μm. AC/Pulsed measured data are shown with closed/open squares. Simulated and modeled data are shown by crosses and lines, respectively. The inset in (a) analogously shows the dependence of the normalized thermal resistance as a function of the gate width.

average the temperature in the channel area, the device temperature increment, $\Delta T$, was calculated from the average temperature in the channel region (60 nm region in depth just under the gate area), as in [15]. Thus, the simulated thermal resistance is given by $\Delta T/(Q \times W)$, where $W$ is expressed in millimeters. As an example, the structure for 3-D thermal simulation of the reference device is shown in Fig. 5, where the temperature profile and corresponding cross-sectional view through the gate are represented, together with the temperature distribution at the barrier/channel heterojunction. The simulated thermal resistance was 147.5 °C/W, which is in good agreement with the measured data.

### *B. Results and Modeling*

The dependence of the thermal resistance of GaN-based HEMTs as a function of the gate width, obtained with the AC/pulsed method, is shown with closed/open symbols in Fig. 6(a). The inset in Fig. 6(a) shows the corresponding dependences of the normalized thermal resistance (thermal

resistance times the gate width). Analogously, the dependence of the thermal resistance on gate length is shown in Fig. 6(b).

Both tendencies with gate width and gate length of the thermal resistance were properly simulated as shown by crosses in Figs. 6(a) and (b), in good agreement with the measured data that is better with those obtained with the pulsed method.

As expected, the thermal resistance significantly decreases when both geometric parameters expand, since more heat flow can be spread out of the device through the terminals. Furthermore, from the inset in Fig. 6(a), the wider the gate, the higher the normalized thermal resistance. This could be attributed to transversal thermal effects, as explained later, which are negligible for a sufficiently high gate width (when normalized thermal resistance tends to be constant).

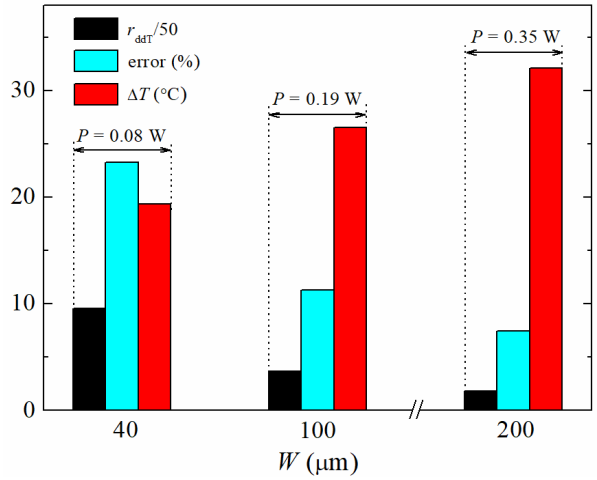
On the other hand, the reduction in thermal resistance as the length of the channel increases, as shown in Fig. 6(b), is evidence that the heat flow through the gate contact becomes more significant. This tendency vanishes for very long channels, when no additional heat flow is dissipated via the gate.

The discrepancy between the thermal resistances obtained with the AC conductance and pulsed methods increases when the gate width diminishes and gate length rises, as shown in Figs. 7(a) and (b), respectively, where the relative errors between the measured data from both methods are represented by vertical blue columns. This dependence of the relative error on the gate geometry could be attributed to a corresponding augmented mismatch between the AC output resistance of the device at high frequencies, $r_{ddT} = 1/g_{ddT}$, and the nominal resistance (50 Ω) at the input ports of the vector network analyzer, as Figs. 7(a) and (b) suggest, where normalized AC output resistances, $r_{ddT}(\Omega)/50$, are shown by vertical black columns. In addition, the predicted device temperature increment, $\Delta T = R_{th}P$, where $P = I_dV_d$ is the power dissipation, diminishes when the gate width/length reduces/rises, which is represented in Figs. 7(a) and (b) with vertical red columns. A reduction in the device temperature increment indicates a minor variation in the conductance with the operation frequency and a minor deviation between the DC and pulsed output conductances, which introduce a greater uncertainty in the measurement of the thermal resistance with both measurement techniques. Herein, the AC conductance technique seems to be precise enough for the HEMTs whose channel is neither narrower than 100 µm nor longer than 3 µm, which are commonly used in RF power applications. The use of higher power dissipation levels could extend some of these limits, but trapping effects could take place as the applied electric field increases [34].

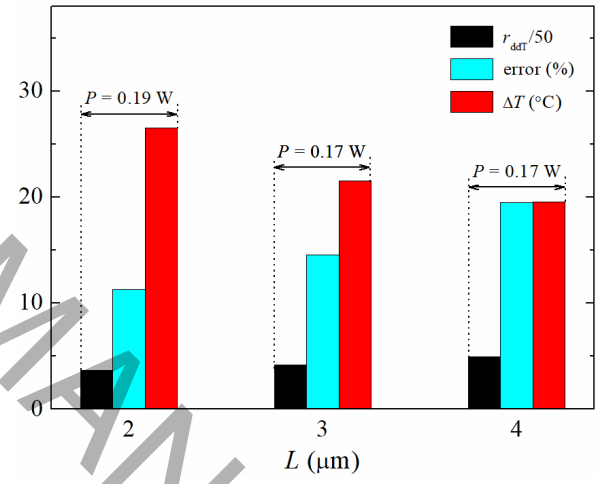
Thus, the obtained thermal resistances can be modeled as in [29]:

$$R_{th} = \frac{R_{tho}}{W+a}\left[1+L_o\left(\frac{1}{L}-\frac{1}{L_{ref}}\right)\right], \quad (4)$$

where $L_{ref}$ is the gate length of the reference device, for which the thermal conductance, $G_{th} = 1/R_{th}$, obeys the linear




(a)




(b)

Fig. 7. Normalized AC output resistance without dynamic SHEs (black columns), relative error for the thermal resistance with both AC conductance and pulsed techniques (blue columns), and device temperature increment due to SHEs (red columns) with (a) gate width, for $L$ = 2 µm and (b) channel length, for $W$ = 100 µm.

TABLE I
PARAMETERS TO MODEL THE DEPENDENCY OF THERMAL RESISTANCE ON DEVICE GEOMETRY WITH THE AC TECHNIQUE

| | |
|---|---|
| $R_{tho}$ (°C-mm/W) | 24.18 |
| $a$ (mm) | 0.07 |
| $L_o$ (µm) | 0.80 |
| $L_{ref}$ (µm) | 2.00 |

dependence $G_{th} = (W + a)/R_{tho}$. The positive thermal conductance at a hypothetical zero device width, $a/R_{tho}$, indicates that heat dissipation from hot channel region is not just parallel to current flow (longitudinal) and vertical through the substrate and terminals, but also transverse via the gate metal or the substrate [35]. This is enhanced by the large peak temperature in the center of the device versus the surface average across the width of the device [23]. This results in a temperature gradient transverse to the current flow, and its contribution to the total heat flow is expected to diminish as the gate width increases. Thus, $R_{tho}$ represents the normalized

thermal resistance for sufficiently wide HEMTs (i.e., when $W >> a$ and transversal thermal dissipation can be neglected). The parameters $R_{tho}$ and $a$ can be determined from the slope and $W$-axis intercept of the gate width dependence of the thermal conductance for the reference device, respectively. Similarly, $L_o$ (to modulate the gate length dependency) can be determined from the $1/L$-axis intercept of the reverse gate length dependence of the thermal resistance. The resulting values for $R_{tho}$, $a$, and $L_o$ are shown in Table I for the AC technique.

Modeled data are shown with solid lines in Figs. 6(a) and (b), showing the expected dependence on gate geometry and agreeing with the AC measured data, with a relative error of ≤10%.

Higher thermal resistances for the GaN-based HEMTs under study were obtained in [29] (35% higher than those obtained with the AC conductance technique). In this case, as in [15], the channel temperature under operation was obtained by measuring the drain current negatively pulsing from various bias conditions at the drain terminal, when self-heating was established through non-zero power dissipation. This could lead to current collapse by trapping effects (the time constant of trap emission is higher than the pulse width, 200 ns), as indicated in [21], resulting in a lower drain current than that due to SHEs and, therefore, a higher thermal resistance.

Finally, it is expected that the AC conductance method can be applied similarly to high-power HEMTs, to extract the thermal resistance without difficulty.

## V. Conclusions

The thermal resistance of GaN-based HEMTs on silicon has been successfully measured using the AC conductance method. Comparable results have been obtained with the pulsed measurement method and 3-D thermal simulations for the HEMTs whose channel is neither narrower than 100 μm nor longer than 3 μm. The dependencies of the thermal resistance on gate geometry (its reduction as both gate width and gate length expand, including narrow width effects) obtained in other technologies were observed and modeled for circuit-design purposes. In the case of the pulsed measurement method, negatively pulsing of the drain voltage has been avoided in order not to overestimate the thermal resistance by trapping effects.

## References


[1] G. Tang, T. c. Chai, and X. Zhang, "Thermal optimization and characterization of SiC-based high power electronics packages with advanced thermal design," *IEEE Trans. Compon. Pack. Manuf. Technol*., vol. 9, no. 5, pp. 854–863, May 2019, doi: 10.1109/TCPMT.2018.2860998.

[2] R. Paschotta, J. Aus der Au, and U. Keller, "Thermal effects in high-power end-pumped lasers with elliptical-mode geometry," *IEEE J. Sel. Top. Quantum Electron*., vol. 6, no. 4, pp. 636–642, July-Aug. 2000, doi: 10.1109/2944.883378.

[3] N. M. Zainuddin, M. S. Abd. Rahman, M. Z. A. Ab. Kadir, N. H. N. Ali, Z. Ali, M. Osman, M. Mansor, A. M. Ariffin, M. S. Abd. Rahman, S. F. M. NOR, and N. A. F. M. NASIR, "Review of Thermal Stress and Condition Monitoring Technologies for Overhead Transmission Lines: Issues and Challenges," *IEEE Access*, vol. 8, pp. 120053–120081, 2020, doi: 10.1109/ACCESS.2020.3004578.

[4] L. Baczkowski, J. Jacquet, O. Jardel, C. Gaquière, M. Moreau, D. Carisetti, L. Brunel, F. Vouzelaud, and Y. Mancuso, "Thermal Characterization Using Optical Methods of AlGaN/GaN HEMTs on SiC Substrate in RF Operating Conditions," ," *IEEE Trans. Electron Devices*, vol. 62, no. 12, pp. 3992–3998, Dec. 2015, doi: 10.1109/TED.2015.2493204.

[5] M. Shrivastava, M. Agrawal, S. Mahajan, H. Gossner, T. Schulz, D. K. Sharma, and V. R. Rao, "Physical insight toward heat transport and an improved electrothermal modeling framework for FinFET architectures," *IEEE Trans. Electron Devices*, vol. 59, no. 5, pp. 1353–1363, May 2012, doi: 10.1109/TED.2012.2188296.

[6] J. Park, M. W. Shin, and C. Lee, "Thermal modelling and measurements of GaN-based HFET devices," *IEEE Electron Device Lett.*, vol. 24, no. 7, pp. 424–426, July 2003, doi: 10.1109/LED.2003.814020.

[7] C. K. Yang, P. Roblin, F. De Groote, S. A. Ringel, S. Rajan, J. P. Teyssier, C. Poblenz, Y. Pei, J. Speck, and U. K. Mishra, "Pulsed-IV Pulsed-RF Cold-FET Parasitic Extraction of Biased AlGaN/GaN HEMTs Using Large Signal Network Analyzer," *IEEE Trans. Microw. Theory Techn*., vol. 58, no. 5, pp. 1077–1088, May 2010, doi: 10.1109/TMTT.2010.2045452.

[8] X. Zhao, Y. Xu, Y. Jia, Y. Wu, R. Xu, J. Li, Z. Hu, H. Wu, W. Dai, and S. Cai, "Temperature-Dependent Access Resistances in Large-Signal Modeling of Millimeter-Wave AlGaN/GaN HEMTs," *IEEE Trans. Microw. Theory Techn*., vol. 65, no. 7, pp. 2271–2278, July 2017, doi: 10.1109/TMTT.2017.2658561.

[9] N. Rinaldi, "Small-signal operation of semiconductor devices including self-heating, with application to thermal characterization and instability analysis," *IEEE Trans. Electron Devices*, vol. 48, no. 2, pp. 323–331, Feb. 2001, doi: 10.1109/16.902734.

[10] S. Makovejev, S. H. Olsen, V. Kilchytska, and J. P. Raskin, "Time and frequency domain characterization of transistor self-heating," *IEEE Trans. Electron Devices*, vol. 60, no. 6, pp. 1844–51, Jun. 2013, doi: 10.1109/TED.2013.2259174.

[11] B. González, R. Rodriguez, and A. Lazaro, "Thermal resistance characterization for multifinger SOI-MOSFETs," *IEEE Trans. Electron Devices*, vol. 65, no. 9, pp. 3626–3632, Sep. 2018, doi: 10.1109/TED.2018.2853799.

[12] K. A. Jenkins, J. Y.-C. Sun, and J. Gautier, "Characteristics of SOI FET's under pulsed conditions," *IEEE Trans. Electron Devices*, vol. 44, no. 11, pp. 1923–1930, Nov. 1997, doi: 10.1109/16.641362.

[13] C. Anghel, R. Gillon, and A. M. Ionescu, "Self-heating characterization and extraction method for thermal resistance and capacitance in HV MOSFETs," *IEEE Electron Device Lett.*, vol. 25, no. 3, pp. 141–143, March 2004, doi: 10.1109/LED.2003.821669.

[14] V. Smirnov, V. Sergeev, A. Gavrikov and A. Kulikov, "Measuring Thermal Resistance of GaN HEMTs Using Modulation Method," *IEEE Trans. Electron Devices*, vol. 67, no. 10, pp. 4112–4117, Oct. 2020, doi: 10.1109/TED.2020.3013509.

[15] J. Joh, J. A. del Alamo, U. Chowdhury, T.-M. Chou, H.-Q. Tserng, and J. L. Jimenez, "Measurement of channel temperature in GaN high-electron mobility transistors," *IEEE Trans. Electron Devices*, vol. 56, no. 12, pp. 2895–2901, Dec. 2009, doi: 10.1109/TED.2009.2032614.

[16] C. Florian, A. Santarelli, R. Cignani, and F. Filicori, "Characterization of the nonlinear thermal resistance and pulsed thermal dynamic behavior of AlGaN–GaN HEMTs on SiC," *IEEE Trans. Microw. Theory Techn*., vol. 61, no. 5, pp. 1879–1891, May 2013, doi: 10.1109/TMTT.2013.2256146.

[17] M. Kuball and J. W. Pomeroy, "A review of Raman thermography for electronic and opto-electronic device measurement with submicron spatial and nanosecond temporal resolution," *IEEE Trans. Device Mater. Rel*., vol. 16, no. 4, pp. 667–684, Dec. 2016, doi: 10.1109/TDMR.2016.2617458.

[18] A. Chini, F. Soci, M. Meneghini, G. Meneghesso, and E. Zanoni, "Deep levels characterization in GaN HEMTs—Part II: Experimental and numerical evaluation of self-heating effects on the extraction of traps activation energy," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3166–3182, Oct. 2013, doi: 10.1109/TED.2013.2278290.

[19] K. R. Bagnall, O. I. Saadat, S. Joglekar, T. Palacios, and E. N. Wang, "Experimental characterization of the thermal time constants of GaN HEMTs via micro-Raman thermometry," *IEEE Trans. Electron Devices*, vol. 64, no. 5, pp. 2121–2128, May 2017, doi: 10.1109/TED.2017.2679978.

[20] Y. Shan, W. Gao, Z. Huang, W. Kuang, Z. Wu, and B. Zhang, "Test Methods and Principles of Thermal Resistance for GaN HEMT Power Devices," in Proc. *21st Int. Conf. on Electron. Packag. Technol. (ICEPT)*, Guangzhou Science City, China, Aug. 2020, pp. 1–4, doi: 10.1109/ICEPT50128.2020.9202571.

[21] R. Sommet, G. Mouginot, R. Quere, Z. Ouarch, and M. Camiade, "Thermal modeling and measurements of AlGaN/GaN HEMTs including thermal boundary resistance," *Microelectron. J.*, vol. 43, no. 9, pp. 611–617, Sept. 2012, doi: 10.1016/j.mejo.2011.07.009.

[22] B. K. Schwitter, A. E. Parker, A. P. Fattorini, S. J. Mahon and M. C. Heimlich, "Study of Gate Junction Temperature in GaAs pHEMTs Using Gate Metal Resistance Thermometry," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3358–3364, Oct. 2013, doi: 10.1109/TED.2013.2278704.

[23] G. Pavlidis, S. Pavlidis, E. R. Heller, E. A. Moore, R. Vetury, and S. Graham, "Characterization of AlGaN/GaN HEMTs Using Gate Resistance Thermometry," *IEEE Trans. Electron Devices*, vol. 64, no. 1, pp. 78–83, Jan. 2017, doi: 10.1109/TED.2016.2625264.

[24] A. Cutivet, G. Pavlidis, B. Hassan, M. Bouchilaoun, C. Rodriguez, A. Soltani, S. Graham, F. Boone, and H. Maher, "Scalable Modeling of Transient Self-Heating of GaN High-Electron-Mobility Transistors Based on Experimental Measurements," *IEEE Trans. Electron Devices*, vol. 66, no. 5, pp. 2139–2145, May 2019, doi: 10.1109/TED.2019.2906943.

[25] J. Bremer, D. Y. Chen , A. Malko, M. Madel, N. Rorsman, S. E. Gunnarsson, K. Andersson, T. M. J. Nilsson, P. E. Raad, P. L. Komarov, T. L. Sandy, and M. Thorsell, "Electric-Based Thermal Characterization of GaN Technologies Affected by Trapping Effects," *IEEE Trans. Electron Devices*, vol. 67, no. 5, pp. 1952-1958, May 2020, doi: 10.1109/TED.2020.2983277.

[26] A. M. Darwish, A. J. Bayba, and H. A. Hung, "Thermal resistance calculation of AlGaN-GaN devices," *IEEE Trans. Microw. Theory Tech.,* vol. 52, no. 11, pp. 2611–2620, Nov. 2004, doi: 10.1109/TMTT.2004.837200.

[27] A. K. Sahoo, N. K. Subramani, J.-C. Nallatamby, R. Sommet, R. Quéré, N. Rolland, and F. Medjdoub, "Thermal analysis of AlN/GaN/AlGaN HEMTs grown on Si and SiC substrate through TCAD simulations and measurements," in Proc. *11th Eur. Microw. Integr. Circuits Conf. (EuMIC)*, London, U.K., Oct. 2016, pp. 145–148, doi: 10.1109/EuMIC.2016.7777511.

[28] P. Kushwaha, K. B. Krishna, H. Agarwal, S. Khandelwal, J.-P. Duarte, C. Hu, and Y. S. Chauhan, "Thermal resistance modeling in FDSOI transistors with industry standard model BSIM-IMG," *Microelectron. J.*, vol. 56, pp. 171–176, Oct. 2016, doi: 10.1016/j.mejo.2016.07.014.

[29] B. González, C. De Santi, F. Rampazzo, M. Meneghini, A. Nunez, E. Zanoni, and G. Meneghesso, "Geometric modeling of thermal resistance in GaN HEMTs on Silicon," *IEEE Trans. Electron Devices*, vol. 67, no. 12, pp. 5408–5414, Dic. 2020, doi: 10.1109/TED.2020.3028358.

[30] L. Di Cioccio, E Morvan, M. Charles, P. Perichon, A. Torres, F. Ayel, D. Bergogne, Y. Baines, M. Fayoll, R. Escoffier, W. Vandendaele, D. Barranger, G. Garnier, L. Mendizabal, B. Thollin, and M. Plissonnier, "From epitaxy to converters topologies what issues for 200 mm GaN/Si?," in *IEDM Tech. Dig.*, Washington, DC, USA, Dec. 2015, pp. 16.5.1–16.5.4, doi: 10.1109/IEDM.2015.7409712.

[31] G. Pailloncy and J. P. Raskin, "New de-embedding technique based on Cold-FET measurement," in *Proc. European Microwave Integrated Circuits Conf.*, Manchester, U.K., Sept. 2006, pp. 460–463, doi: 10.1109/EMICC.2006.282682.

[32] *Sentaurus Device User Guide*, Version N-2017.09, Synopsys, Mountain View, CA, USA, 2019.

[33] S. Rajasingam, J. W. Pomeroy, M. Kuball, M. J. Uren, T. Martin, D. C. Herbert, K. P. Hilton, and R. S. Balmer, "Micro-Raman temperature measurements for electric field assessment in active AlGaN-GaN HFETs," *IEEE Electron Device Lett.*, vol. 25, no. 7, pp. 456–458, July 2004, doi: 10.1109/LED.2004.830267.

[34] C. Potier, A. Martin, M. Campovecchio, S. Laurent, R. Quere, J.C. Jacquet, O. Jardel, S. Piotrowicz, and S. Delage, "Trap characterization of microwave GaN HEMTs based on frequency dispersion of the output-admittance," in *Proc. 9th Eur. Microw. Integr. Circ. Conf.*, Oct. 2014, pp. 464–467, doi: 10.1109/EUMIC.2014.6997893.

[35] S. Lee, R. Wachnik, P. Hyde, L. Wagner, J. Johnson, A. Chou, A. Kumar, S. Narasimha, T. Standaert, B. Greene, T. Yamashita, J. Johnson, K. Balakrishnan, H. Bu, S. Springer, G. Freeman, W. Henson, and E. Nowak, "Experimental analysis and modeling of self heating effect in dielectric isolated planar and fin devices," in Proc. IEEE Symp. VLSI Technol., Kyoto, Japan, Jun. 2013, pp. T248–T249.