Gate Length-Dependent Thermal Impedance Characterization of PD-SOI MOSFETs

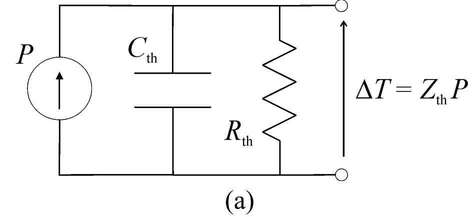
Benito González, José M. Cabrera, and Antonio Lázaro, *Senior Member, IEEE*

***Abstract*—Thermal impedance is required to describe static and fast dynamic thermal behavior in silicon-on-insulator (SOI) devices. This study presents an empirical physical model, which accounts for gate length, for calculating the thermal impedance of multi-finger partially depleted (PD) SOI MOSFETs at room temperature. For the first time, the parameters of the model are obtained from measurements of AC conductance and the characteristic thermal frequency determination. The model shows decreasing thermal resistance and linearly augmented thermal capacitance with increasing gate length from 0.18 to 2.50 µm. Thus, thermal time constants of ~760 ns, extracted from a variety of gate lengths, are correctly predicted.**

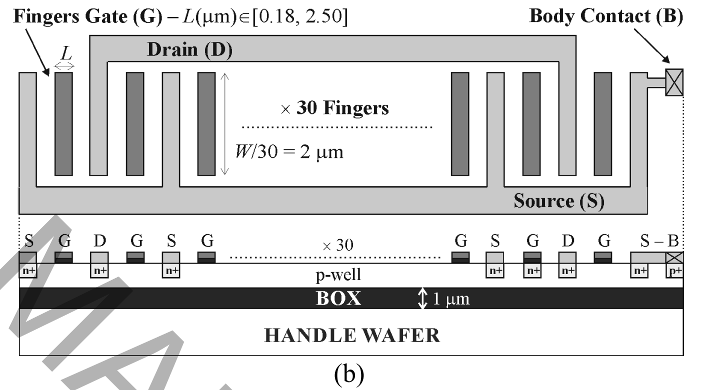
Index Terms—**Electrothermal characterization, model, SOI MOSFET, thermal impedance.**

I. Introduction

The typical thermal model for the temperature rise in devices induced by self-heating effects (SHEs) consists of an equivalent circuit with the thermal resistance, R_{th}, and capacitance, C_{th}, connected in parallel (see Fig. 1(a)). The first-order R_{th}–C_{th} network was demonstrated to be sufficient for the thermal modeling of silicon-on-insulator (SOI) MOSFETs with intermediate gate lengths [1], [2]. The thermal resistance, which has been extensively studied in SOI MOSFETs [3]−[5], models the static thermal performance of a device. Meanwhile, the thermal capacitance is necessary to describe the fast dynamic thermal behavior in SOI devices subjected to abrupt changes in power generation [6], [7]. Thus, the temperature rise in the device channel, ΔT, is given by $Z_{th}P$, where P is the thermal power dissipated in the device ($P \cong V_d I_d$, neglecting gate current losses) and Z_{th}, with $1/Z_{th} = 1/R_{th} + j\omega C_{th}$, its thermal impedance. This thermal model maintains a high degree of simplicity, which is useful in the context of compact model development for circuit simulators. Furthermore, electrothermal simulations can easily be performed based on a thermal-electrical analogy, by introducing an internal temperature node into the device. This node is connected to ground through the thermal impedance, and the nodal voltage is actually the temperature rise in the device channel when the current flowing through the thermal impedance equals the power dissipated in the device, that can be obtained during the circuit simulation using a controlled current source of value $V_d I_d$.



(a)



(b)

Fig. 1. (a) Equivalent circuit for SHEs in devices. (b) Top and cross-sectional views of the structure of the devices under study (drawings not to scale). The central fingers and the corresponding source and drain terminals are assumed (not shown).

The thermal time constant, τ_{th}, which characterizes the thermal transient response to pulsed measurements [8], can be easily determined as $R_{th}C_{th}$. Alternatively, the characteristic thermal frequency, $f_{th} = 1/(2\pi R_{th}C_{th})$, can be used to determine the thermal frequency response.

The gate width is usually the only geometrical parameter considered during the thermal modeling of SOI MOSFETs [4], [9]. However, it has been demonstrated that the length of the channel has a non-negligible impact on the thermal impedance [10] and must be considered for precise compact modeling [11].

The thermal resistance of SOI MOSFETs reduces as the length of the channel increases [10] when the heat flow through the gate contact becomes more significant. This tendency vanishes for very long channels when self-heating

This work was supported by the Spanish MEC under Project NextIOT-RTI2018-096019-B-C31.

B. González and J. M. Cabrera are at the Institute for Applied Microelectronics, Universidad de Las Palmas de Gran Canaria, Campus Universitario de Tafira, Las Palmas, CO 35017, Spain (e-mail: benito@iuma.ulpgc.es and jcabrera@iuma.ulpgc.es).

A. Lázaro is at the Departament of Electronic, Electrical and Automatic Engineering, Universitat Rovira i Virgili, Escola Tècnica Superior d'Enginyeria, Av. Dels Països Catalans 26, Tarragona, CO 43007 Spain (e-mail: antonioramon.lazaro@urv.cat).

ACCEPTED MANUSCRIPT
THE COPYRIGHT

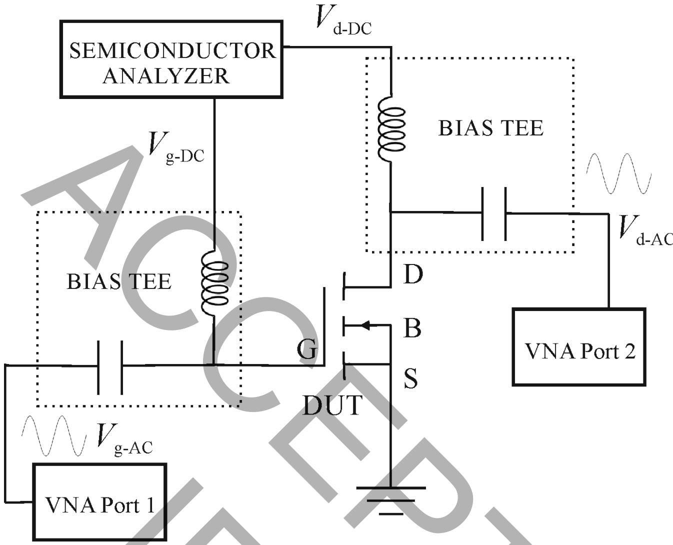


Fig. 2. Schematic of an AC measurement system for the device under test.

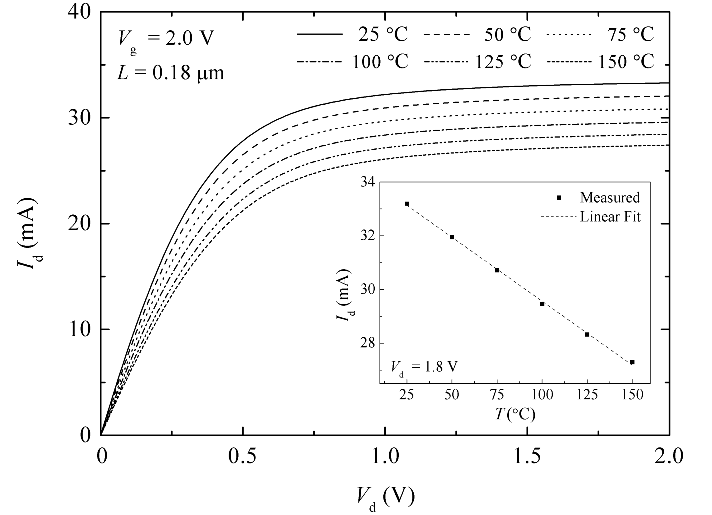


Fig. 3. Measured output characteristics at different substrate temperatures for a multi-finger PD-SOI MOSFET with a gate length of 0.18 μm and V_g = 2 V. Inset: resulting linear temperature dependence of the drain current for V_d = 1.8 V.

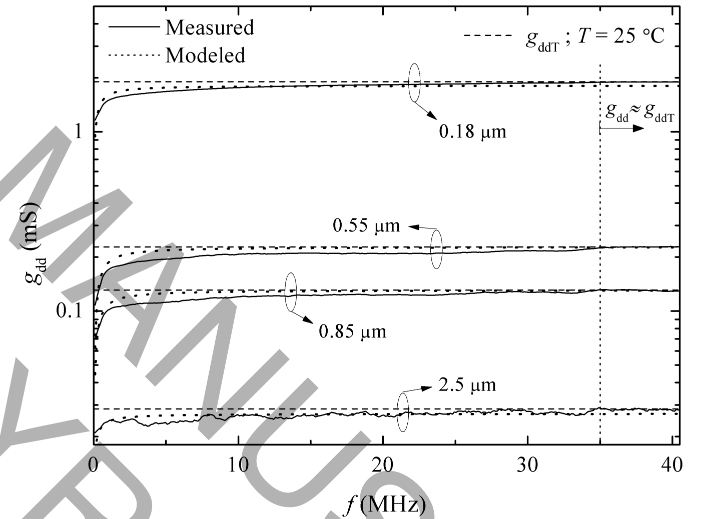


Fig. 4. Measured (with solid lines) and modeled (with dotted lines) conductance frequency response at room temperature for multi-finger PD-SOI MOSFETs with different gate lengths of 0.18, 0.55, 0.85 and 2.50 μm for V_g = 2 V and V_d = 1.8 V.

can be neglected. No gate length dependence of the thermal resistance is also expected for short channels when the heat flow through the gate is negligible (the source and drain contacts do not shrink) [11].

In addition, when SOI technology is used, the very low thermal conductivity of the SiO_2 buried oxide (BOX) layer significantly impedes heat transfer towards the substrate, particularly for thicknesses greater than 100 nm [5]. In this case, most of the self-heating spreads out of the device through source and drain terminals for short channels.

The thermal capacitance is a volumetric physical property. Therefore, it is expected to increase with the length of the channel, similarly to the linear increase observed with the gate width [10], [12]. Nevertheless, to the best of our knowledge, this dependence of the thermal capacitance of SOI MOSFETs has not yet been extracted using the measured characteristic thermal frequency or modeled.

In this study, the thermal impedance of multi-finger partially depleted (PD) SOI MOSFETs with different gate lengths is obtained with a methodology based on the AC technique [3] and the characteristic thermal frequency determined through the conductance frequency response [1], [12]. Additionally, a model for the gate length dependence of the thermal impedance is proposed, with the aim of its implementation in circuit simulators.

The PD-SOI MOSFETs under consideration here are described in Section II. The experimental setup used for their thermal impedance characterization is detailed in Section III. Section IV is devoted to thermal impedance characterization and modeling, and the validation of the model and its limitations are discussed in Section V. Finally, the conclusions are presented in Section VI.

II. Fabricated Devices

In order to study the thermal impedance as a function of the gate length, L, nine PD-SOI N-channel MOSFETs were fabricated with gate length varying from 0.18 to 2.50 μm and 1-μm-thick BOX, using XT018 0.18 μm HV SOI CMOS technology (by XFAB). The transistors, with a threshold voltage of 0.6 V, were body tied to prevent the floating-body effect and embedded in ground-signal-ground on-wafer test structures. To enhance self-heating, multi-finger devices composed of 30 parallel fingers, with each finger being 2 μm wide for a total gate width, W, of 60 μm, were designed. Top and cross-sectional views of the structure of the devices under study are shown in Fig. 1(b), and the gate dimensions and BOX thickness have been labeled.

III. Experimental Setup

On-wafer measurements were performed with a Cascade Summit 9000 probe station. As indicated in Fig. 2 for the experimental setup, the S parameters were measured at room temperature from 100 kHz to 40 MHz with an

ACCEPTED MANUSCRIPT IEEE COPYRIGHT

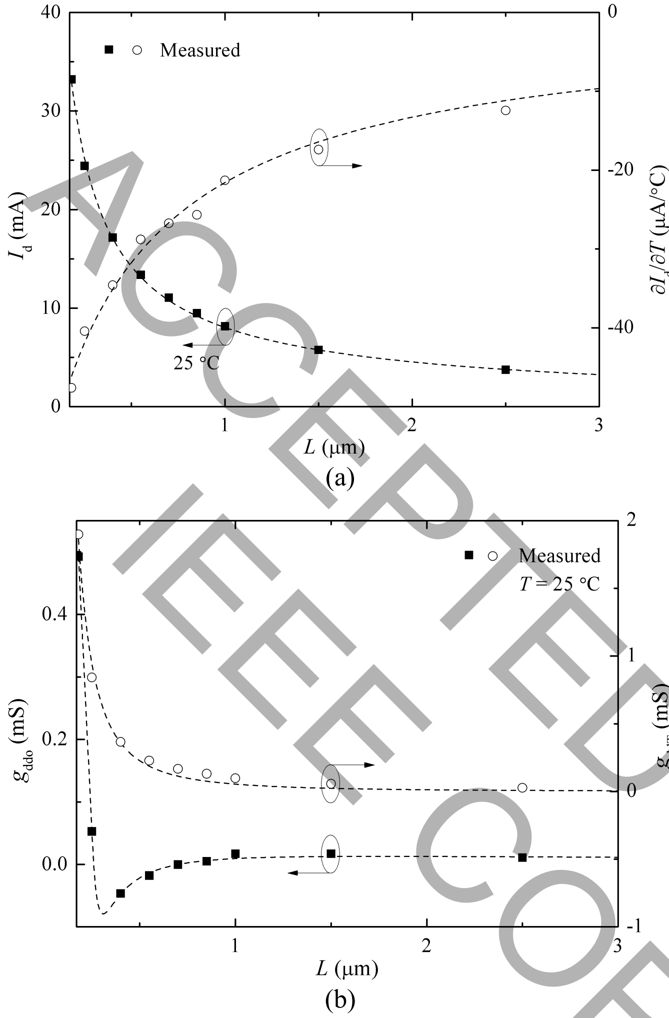


Fig. 5. (a) Drain current (left axis) and its slope with temperature (right axis) and (b) DC conductance (left axis) and conductance without dynamic self-heating (right axis), as a function of the gate length for multi-finger PD-SOI MOSFETs, extracted from measurements (scattered) and corresponding tendencies (dashed lines) for $V_g = 2$ V and $V_d = 1.8$ V.

Agilent N9913A vector network analyzer and Cascade ground-signal-ground microprobes. An Agilent B1500A semiconductor analyzer made the device under test operate in the saturation regime, with DC gate and drain voltages of $V_g = 2$ V and $V_d = 1.8$ V, respectively, to enhance SHEs [9].

In order to calibrate the measurement system, the short-open-load-through method was implemented in a previous step and the pad-to-device parasitic elements were de-embedded with the open-short-through de-embedding technique [13].

The DC parameters were measured with the Agilent B1500A semiconductor analyzer. For obtaining the temperature dependence of the drain current, the transistors were placed on a hotplate. The substrate temperature was changed from 25 to 150 °C in steps of 25 °C.

IV. Thermal Impedance Characterization and Modeling

A. Thermal Resistance

According to the AC conductance technique for MOSFETs [3], the thermal resistance of a device is given by:

$$R_{th} = \frac{g_{ddo} - g_{ddT}}{\frac{\partial I_d}{\partial T}\left(V_d\, g_{ddT} + I_d\right)} \quad (1)$$

where g_{ddo} is the DC conductance, g_{ddT} is the conductance at high frequency (with dynamic self-heating removed) and I_d is the drain current.

These parameters were obtained for all devices at the bias considered ($V_g = 2$ V and $V_d = 1.8$ V) in the experimental setup. In the case of g_{ddo} and I_d, these values were extracted from the I_d-V_{ds} curve for $V_g = 2$ V at room temperature ($T = 25$ °C, shown by a solid line in Fig. 3 for $L = 0.18$ μm). Output characteristics at different temperatures (lines in Fig. 3) were used to determine $\partial I_d/\partial T$ at the bias considered from the resulting linear temperature dependence of the drain current (inset in Fig. 3). Finally, the conductance frequency response at room temperature from the *S* parameters (shown by solid lines in Fig. 4 for different gate lengths), $g_{dd}(f)$, was used to extract the value of the conductance without dynamic self-heating, g_{ddT}, at which g_{dd} reaches a plateau (shown with dashed lines). Note that the conductance shows a plateau above 35 MHz for all gate lengths, a result that is consistent with the conductance frequency response observed in [9].

The gate length dependence of the parameters in (1) is represented with symbols in Fig. 5(a) for I_d, left axis, and $\partial I_d/\partial T$, right axis, and (b) for g_{ddo}, left axis, and g_{ddT}, right axis. The corresponding trends are shown with dashed lines. In the case of g_{ddo} and g_{ddT}, an asymptotic response towards a value of zero appears for longer channels. Regarding the g_{ddo}

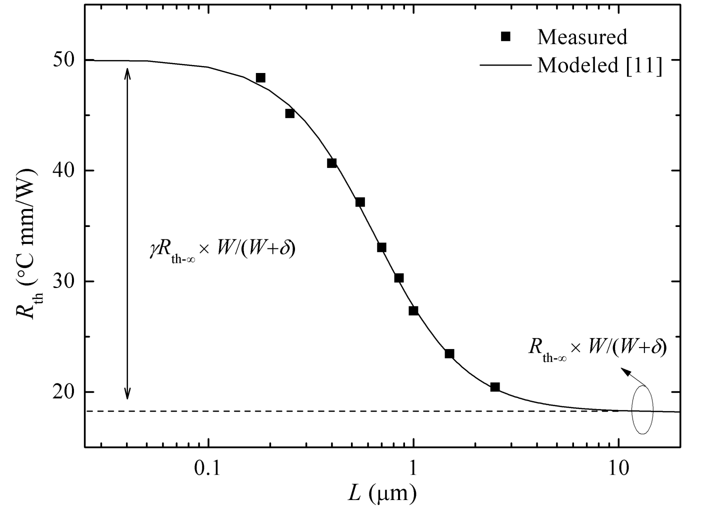


Fig. 6. Thermal resistance per unit width with gate length extracted from measurements (scattered) and modeled (line) for multi-finger PD-SOI MOSFETs.

TABLE I
Parameters for Gate Length Dependence of PD-SOI MOSFET Thermal Impedance

$R_{th\text{-}\infty}$ (°C mm/W)	α	β	γ	δ (μm)	C_{tho} (nJ/°C mm)	m (μm^{-1})	φ (μm)
18.24	2.35	1.96	1.76	0.19	16.27	0.66	-2.86

ACCEPTED MANUSCRIPT
IEEE COPYRIGHT

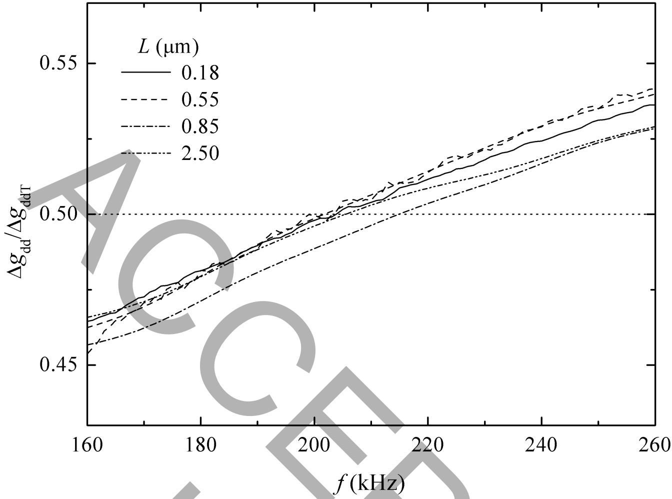


Fig. 7. $\Delta g_{dd}/\Delta g_{ddT}$ frequency response at room temperature for multi-finger PD-SOI MOSFETs with different lengths of the channel of 0.18, 0.55, 0.85 and 2.50 μm for $V_g = 2$ V and $V_d = 1.8$ V.

response, two opposite tendencies for the drain current occur for shorter gate lengths. Firstly, short-channel effects (SCEs), such as drain-induced barrier lowering (DIBL) and the channel-length modulation (CML) effect, affect the output characteristics, causing the drain current to increase with drain bias and lowering the transistor output resistance [14]. Experiments reveal that DIBL increases with temperature [15]. Secondly, SHEs, which are more pronounced for shorter gate lengths, cause the drain current to decrease and hence increase the transistor output resistance. Thus, for reduced lengths of the channel it seems that SCEs prevail over SHEs, resulting in a positive output conductance. As the gate length increases, SCEs disappear faster than SHEs when g_{ddo} is negative, as in [3]. Finally, for longer devices, SCEs and SHEs vanish and the output conductance tends to zero.

The measured thermal resistance per unit width as a function of the gate length is shown in Fig. 6 with symbols. Similar values for the normalized thermal resistances were obtained in [2], [9], [11] and [16].

The obtained thermal resistances per unit width can be modeled as in [11] for fully depleted (FD) SOI MOSFETs. When the gate width dependence observed in [9] is incorporated, we obtain the following expression:

$$R_{th} = R_{th\text{-}\infty}\left(1+\frac{\gamma}{1+\alpha L^{\beta}}\right)\frac{W}{W+\delta} \tag{2}$$

where L and W are expressed in microns and $R_{th\text{-}\infty} \times W/(W+\delta)$ represents the thermal resistance per unit width for very long gates ($L > 6$ μm when self-heating is negligible). This must be increased by γ times $R_{th\text{-}\infty} \times W/(W+\delta)$ to predict the thermal resistance saturation for short channel devices ($L < 40$ nm, as shown in Fig. 6, when most self-heating is spread out of the device through the source and drain terminals). α, β and δ are technology-dependent fitting parameters. The first two of these determine the gate length dependence for intermediate lengths of the channel, while the third (in microns) determines the gate width dependence for narrow channels [9]. Their values are summarized in Table I.

The modeled thermal resistance per unit width is represented with a solid line in Fig. 6, showing the expected dependence and agreeing with the measured data, achieving a relative error of ≤10%.

B. Thermal Capacitance

Once the thermal resistance has been obtained for all multi-finger PD-SOI MOSFETs, the corresponding thermal capacitance is given by:

$$C_{th} = \frac{1}{2\pi f_{th} R_{th}} \tag{3}$$

where f_{th} is the characteristic thermal frequency, for which the conductance is equal to the average of the DC conductance, g_{ddo}, and the conductance without dynamic self-heating, g_{ddT} [1], [12]. Therefore:

$$g_{dd}(f_{th}) = \frac{g_{ddo} + g_{ddT}}{2} \tag{4}$$

or alternatively:

$$\frac{\Delta g_{dd\text{-}th}}{\Delta g_{ddT}} = \frac{1}{2} \tag{5}$$

where $\Delta g_{dd\text{-}th} = g_{dd}(f_{th}) - g_{ddo}$ and $\Delta g_{ddT} = g_{ddT} - g_{ddo}$.

The measured $\Delta g_{dd}/\Delta g_{ddT}$ frequency response at room temperature, whith $\Delta g_{dd} = g_{dd}(f) - g_{ddo}$, is represented by lines in Fig. 7 for different gate lengths. The f_{th} is extracted from the dotted line, when $\Delta g_{dd}/\Delta g_{ddT} = 0.5$. The data are smoothed to eliminate noise, especially for longer channels. This noise for longer channels can be attributed firstly to a conductance decrement with values much lower than the nominal conductance (20 mS) at the input ports of the vector network analyzer and, secondly, to a minor variation of the conductance with the operation frequency due to the descent of self-heating, as the length of the channel increases (compare g_{dd} for $L = 0.18$ and 2.50 μm in Fig. 4). In fact, for multi-finger PD-SOI MOSFETs with a gate length of 4 μm or higher, neither the characteristic thermal frequency nor the conductance plateau could be observed.

The resulting characteristic thermal frequency seems not to depend on the length of the channel, maintaining its value in the frequency range of 200−215 kHz (see Fig. 7). Once the characteristic thermal frequency has been extracted, considering (3), the gate length dependence of the thermal capacitance per unit width in multi-finger PD-SOI MOSFETs was obtained, as indicated in Fig. 8 with symbols. Similar normalized thermal capacitances (1–27 nJ/°C mm) were obtained in [1], [10] and [12] for RF SOI MOSFETs and 236 nJ/°C mm in [16] for FinFETs.

Thus, the thermal capacitance per unit width can be linearly modeled with the gate length, as expected. When the gate width dependence observed in [12] is incorporated, we obtain the following expression:

ACCEPTED MANUSCRIPT

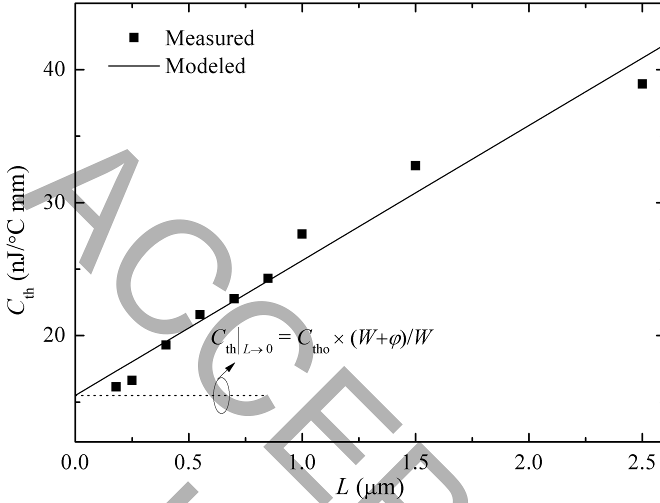


Fig. 8. Thermal capacitance per unit width as a function of gate length extracted and modeled for multi-finger PD-SOI MOSFETs (with symbols and line, respectively).

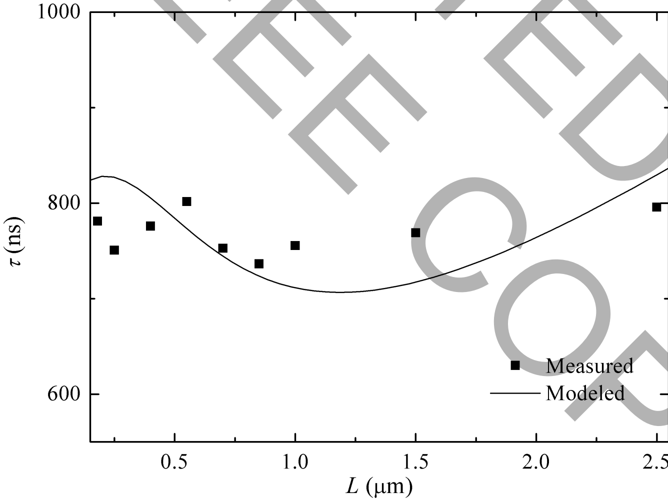


Fig. 9. Thermal time constant extracted from measurements (scattered) and modeled (line) as a function of the length of the channel for multi-finger PD-SOI MOSFETs.

$$C_{th} = C_{tho}(1 + mL)\frac{W+\varphi}{W} \tag{6}$$

where $C_{tho} \times (W+\varphi)/W$ represents the thermal capacitance per unit width at a hypothetical zero gate length (when extrinsic elements determine the thermal performance of the device, as contacts do not scale with the gate length). The proportionality constant m and φ (in microns, which accounts for the thermal capacitance of narrow devices [12]) are technology-dependent fitting parameters. Their values are indicated in Table I and the modeled data are shown with a line in Fig. 8. The relative error between the modeled and measured data is lower than 8.5% in all cases.

Finally, accounting for the measured and modeled data for the thermal resistance and capacitance, Fig. 9 compares the measured (with symbols) and modeled (with line) thermal time constant, $\tau_{th} = R_{th}C_{th}$, for multi-finger PD-SOI MOSFETs, as a function of the length of the channel. Comparable results were obtained in [1]−[3], [12], [16] and [17] for other device technologies. For the transistors under study, the measured thermal time constant does not vary significantly. The modeled data show a maximum relative error of 7.9% with respect to the average thermal time constant of 760 ns. Consistently, a respective characteristic thermal frequency, $1/2\pi\langle\tau_{th}\rangle$, of 209 kHz results in the range of gate lengths under study.

V. Validation and Limitations

This first attempt at modeling the dependence on the gate length of the thermal capacitance of PD-SOI MOSFETs allows for a complete determination of their thermal impedance for circuit simulations. Furthermore, only the conductance frequency response, together with the measured characteristic thermal frequency, was used to obtain C_{th} for PD-SOI MOSFETs.

The resulting modeled conductance frequency response can be evaluated as in [3]:

$$g_{dd} \approx g_{ddT} + Re(Z_{th})\frac{\partial I_d}{\partial T}\left(V_d\, g_{ddT} + I_d\right) \tag{7}$$

which is shown in Fig. 4 with dotted line. A good agreement between modeled and measured output conductance has been obtained, with an average relative error lower than 6.5% in all transistors.

The measured characteristic thermal frequency was obtained based on the assumption of a single thermal time constant, which is convenient for compact modeling and valid for PD-SOI MOSFETs with the gate lengths under consideration [1], [2]. However, this assumption may fail in ultra-scaled devices with a gate length on the order of dozens of nanometers. This was the case for FinFETs in [1], which had a gate length of 14 nm, indicating the existence of a second thermal time constant, and for FD-SOI MOSFETs in [18], which had a gate length of 20 nm, and for which a fourth-order thermal network needed to be employed.

Regarding the gate width dependence of the thermal impedance of PD-SOI MOSFETs, no physical limitations of the model are expected for typical devices, as described in [9], [12], where the gate width ranged between 10 and 60 µm.

Finally, it must be pointed out that the AC technique allows for the identification of different factors (floating body, SHEs, substrate effects, and gate resistance) that affect the variation in the output conductance with frequency, due to different time constants [3]. Thus, the conductance frequency response can be partially masked by other effects than SHEs, and this should be avoided.

To minimize the floating body effect, which appears as augmented conductance at low frequencies, the transistors were body tied [3]. The increase in conductance due to gate resistance is observed in the gigahertz range [9], which is outside the scope of this work. Lastly, substrate effects result in an augmented conductance above 100 MHz [3], [18], at higher frequencies than those at which the conductance reaches a plateau (from 35 to 40 MHz, as shown in Fig. 4). In

ACCEPTED MANUSCRIPT
IEEE COPYRIGHT

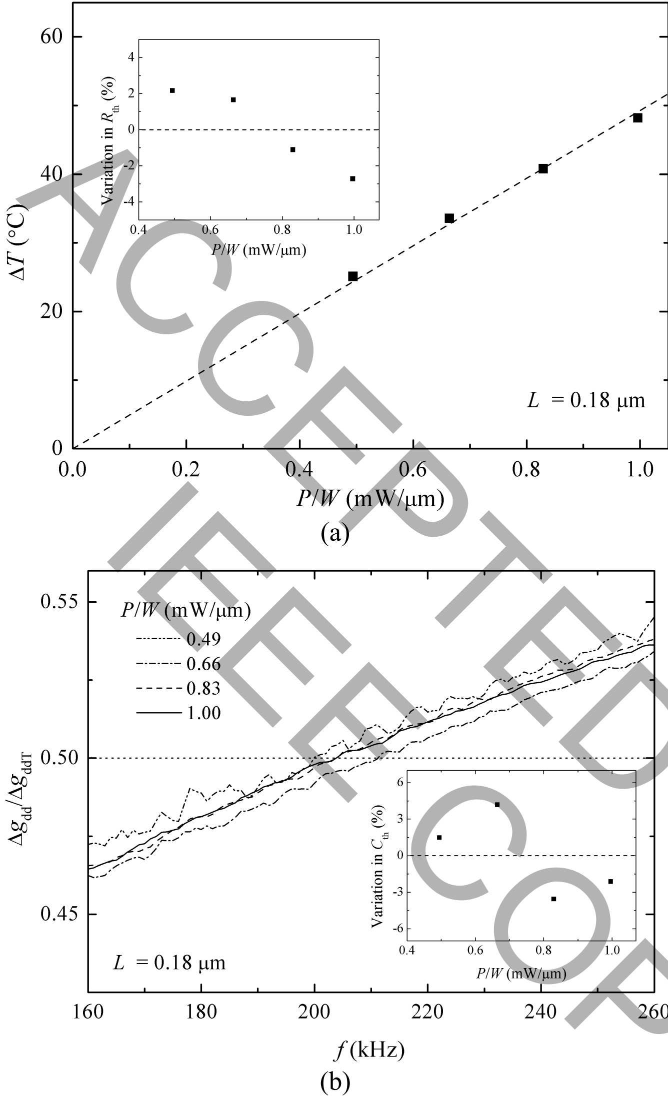


Fig. 10. (a) Extracted temperature rise versus dissipated power, normalized with respect the gate width (60 µm). Inset: Corresponding variation of the thermal resistance. (b) $\Delta g_{dd}/\Delta g_{ddT}$ frequency response for different normalized power dissipations. Inset: Variation of the thermal capacitance with normalized power dissipation.

addition, it is known that substrate effects are relatively weak compared with SHEs with thick BOX layers (1 µm thick in our case).

To demonstrate the non-dependence of the thermal impedance on bias conditions, different power dissipations ranging from ~0.5 to 1 mW/µm were considered in the saturation regime (with V_d = 1.8 V to enhance SHEs), and the gate voltage was varied from 1.4 to 1.8 V in steps of 0.2 V.

The resulting normalized power dissipation dependence of the extracted temperature rise is shown in Fig. 10(a) by the symbols, for the PD-SOI MOSFET with a gate length of 0.18 µm. As expected, a linear dependence is observed (shown by the dashed line), with null temperature rise for zero power dissipation. An average thermal resistance of 49.7 °C mm/W was obtained with a maximum variation of 2.7% (shown in the inset to Fig. 10(a), where the measured variation in R_{th} with normalized power dissipation is represented by symbols. The median R_{th} shown by the dashed line represents a null variation). Regarding the corresponding thermal capacitance, Fig. 10(b) shows (as lines) the resulting measured $\Delta g_{dd}/\Delta g_{ddT}$ frequency response for the different normalized power dissipations, which is similar to that observed when varying the gate length (compare Figs. 7 and 10(b)). In both cases, analogous characteristic thermal frequencies are extracted. An average thermal capacitance of 15.8 nJ/°C mm was found, with a maximum variation of 4.8% (shown in the inset to Fig. 10(b), where the measured variation in C_{th} with normalized power dissipation is represented by symbols. The median C_{th} shown by the dashed line represents a null variation).

There was also no evidence of the dependence on the power dissipation of the thermal impedance of the rest of the devices (the plateau observed at the conductance frequency response is attributed to SHEs). Thus, the model presented here for the thermal impedance of PD-SOI MOSFETs is expected to be valid for the biasing conditions recommended by the fabricant (i.e. up to 2 V).

VI. Conclusions

The thermal impedance of multi-finger PD-SOI MOSFETs, when varying the gate length from 0.18 to 2.50 µm, has been successfully measured for the first time using the AC conductance method, together with the determination of the characteristic thermal frequency. The dependences on the gate length of the thermal resistance and capacitance, at room temperature, have been also modeled for circuit-design purposes. For the thermal capacitance, a linear gate length dependence ($\propto$ 10.2 nJ/°C mm) has been modeled for the first time, with an expected inferior limit of 15.5 nJ/°C mm for ultra-short devices, when extrinsic elements determine the device thermal performance. In addition, the measured thermal time constants have been correctly predicted, showing no relevant gate length dependence and an average value of 760 ns. Finally, the methodology described here is based on the use of first-order thermal networks. For lengths of the channel on the order of dozens of nanometers, an extended order thermal network may be necessary for a proper thermal characterization of PD-SOI MOSFETs, and this will form the subject of future work.

References

[1] U. S. Kumar and V. R. Rao, "A novel TCAD-based thermal extraction approach for nanoscale FinFETs," IEEE Trans. Electron Devices, vol. 64, no. 3, pp. 1404–1407, Mar. 2017. doi: 10.1109/TED.2017.2657626.

[2] W. Jin, W. Liu, S. K. H. Fung, P. C. H. Chan, and C. Hu, "SOI thermal impedance extraction methodology and its significance for circuit simulation," *IEEE Trans. Electron Devices*, vol. 48, no. 4, pp. 730–736, Apr. 2001, doi: 10.1109/16.915707.

[3] S. Makovejev, S. H. Olsen, V. Kilchytska, and J. P. Raskin, "Time and frequency domain characterization of transistor self-heating," *IEEE Trans. Electron Devices*, vol. 60, no. 6, pp. 1844–51, Jun. 2013, doi: 10.1109/TED.2013.2259174.

[4] S. Lee, R. Wachnik, P. Hyde, L. Wagner, J. Johnson, A. Chou, A. Kumar, S. Narasimha, T. Standaert, B. Greene, T. Yamashita, J. Johnson, K. Balakrishnan, H. Bu, S. Springer, G. Freeman, W. Henson, and E. Nowak, "Experimental analysis and modeling of self

ACCEPTED MANUSCRIPT
IEEE COPYRIGHT

heating effect in dielectric isolated planar and fin devices," in *Proc. IEEE Symp. VLSI Technol.*, Kyoto, Japan, Jun. 2013, pp. T248–T249.

[5] M. Shrivastava, M. Agrawal, S. Mahajan, H. Gossner, T. Schulz, D. K. Sharma, and V. R. Rao, "Physical insight toward heat transport and an improved electrothermal modeling framework for FinFET architectures," *IEEE Trans. Electron Devices*, vol. 59, no. 5, pp. 1353–1363, May 2012, doi: 10.1109/TED.2012.2188296.

[6] J. Lin, M. Shen, M.-C. Cheng, and M. L. Glasser, "Efficient thermal modeling of SOI MOSFETs for fast dynamic operation," *IEEE Trans. Electron* Devices, vol. 51, no. 10, pp. 1659–1666, Oct. 2004, doi: 10.1109/TED.2004.835994.

[7] K. A. Jenkins, J. Y.-C. Sun, and J. Gautier, "Characteristics of SOI FET's under pulsed conditions," *IEEE Trans. Electron Devices*, vol. 44, no. 11, pp. 1923–1930, Nov. 1997. doi: 10.1109/16.641362.

[8] A. J. Scholten, G. D. J. Smit, R. M. T. Pijper, L. F. Tiemeijer, H. P. Tuinhout, J.-P. J. van der Steen, A. Mercha, M. Braccioli, and D. B. M. Klaassen, "Experimental assessment of self-heating in SOI FinFETs," *in Proc. IEEE IEDM*, Baltimore, MD, USA, 2009, pp. 1–4, doi: 10.1109/IEDM.2009.5424362.

[9] B. González, R. Rodríguez, and A. Lázaro, "Thermal resistance characterization for multifinger SOI-MOSFETs," *IEEE Trans. Electron Devices*, vol. 65, no. 9, pp. 3626–3632, Sep. 2018, doi: 10.1109/TED.2018.2853799.

[10] Z. Chen , L. Sun, J. Liu , G. Su, and W. Zhou, "Investigation of geometry dependence of thermal resistance and capacitance in RF SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 65, no. 10, pp. 4232–7, Oct. 2018, doi: 10.1109/TED.2018.2863022.

[11] P. Kushwaha, K. B. Krishna, H. Agarwal, S. Khandelwal, J.-P. Duarte, C. Hu, and Y. S. Chauhan, "Thermal resistance modeling in FDSOI transistors with industry standard model BSIM-IMG," Microelectron. J., vol. 56, pp. 171–176, Oct. 2016, doi: 10.1016/j.mejo.2016.07.014.

[12] B. González, B. Aja, E. Artal, A. Lázaro, and A. Núñez, "Temperature-Dependent Thermal Capacitance Characterization for SOI-MOSFETs," *IEEE Trans. Electron Devices*, vol. 66, no. 10, pp. 4120–4125, Oct. 2019, doi: 10.1109/TED.2019.2935500.

[13] I. Gutiérrez, J. Meléndez, J. García, I. Adin, G. Bistue, and J. de No, "Reliability Verification in a Measurement System of Integrated Varactors for RF Applications," *IEEE Lat. Am. Trans.*, vol. 3, no. 4, pp. 15–20, Oct. 2005, doi: 10.1109/TLA.2005.1642424.

[14] G. Hiblot, "DIBL–Compensated Extraction of the Channel Length Modulation Coefficient in MOSFETs," *IEEE Trans. on Electron Devices*, vol. 65, no. 9, pp. 4015–4018, Sept. 2018, doi: 10.1109/TED.2018.2853699.

[15] A. S. N. Pereira, G. de Streel, N. Planes, M. Haond, R. Giacomini, D. Flandre, and V. Kilchytska, "Analysis and modelling of temperature effect on DIBL in UTBB FD SOI MOSFETs," *in Proc. EUROSOI-ULIS*, Vienna, Austria, 2016, pp. 116–119, doi: 10.1109/ULIS.2016.7440066.

[16] S. Makovejev, S. Olsen, and J. Raskin, "RF extraction of self-heating effects in FinFETs," *IEEE Trans. Electron Devices*, vol. 58, no. 10, pp. 3335–3341, Oct. 2011, doi: 10.1109/TED.2011.2162333.

[17] B. M. Tenbroek, W. Redman-White, M. S. L. Lee, R. J. T. Bunyan, and M. J. Uren, "Characterisation of geometry dependence of SOI MOSFET thermal resistance and capacitance parameters," in Proc. IEEE Int. SOI Conf., Fish Camp, CA, USA, Oct. 1997, pp. 114–115. doi: 10.1109/SOI.1997.634959.

[18] L. Nyssens, M. Rack, A. Halder, J.-P. Raskin and V. Kilchytska, "On the Separate Extraction of Self-Heating and Substrate Effects in FD-SOI MOSFET," *IEEE Electron Device Lett.*, vol. 42, no. 5, pp. 665–668, May 2021, doi: 10.1109/LED.2021.3071272.

ACCEPTED MANUSCRIPT
AUTHOR COPYRIGHT