TEST SET-UPS FOR FAST MEASUREMENT OF MONOLITHIC INTEGRATED CIRCUITS FROM ON-WAFER TO SYSTEM. APPLICATION TO A NOVEL GaAs MONOLITHIC TRANSIMPEDANCE AMPLIFIER FOR HIGH SPEED OPTICAL COMMUNICATION SYSTEMS

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ABSTRACT

A fast, accurate and economical method for fully characterizing MMICs from on-wafer to system measurements is presented as well as the corresponding set-ups. The method is applied to the evaluation of a GaAs monolithic transimpedance amplifier for the receiver of a high speed optical communication system. The device was firstly DC and RF measured on-wafer and on-chip in order to test the dispersion as well as for an initial selection of the chips. Using a test-fixture designed for fast on-carrier measurements the selected chips were tested on-carrier. Finally, employing the same carrier but a different test-fixture, optical/electrical measurements were done to evaluate the subsystem behavior. The efficiency of the measurement method is demonstrated in one hand and in the other the test results show that a transimpedance amplifier of excellent performances for high speed rate optical communication systems has been obtained.

Keywords: Test Set-Ups, Test-Fixture, Measurements, On-Wafer, On-Chip, On-Carrier, System, Transimpedance Amplifier, Optical Communication Systems

1. INTRODUCTION

In the validation of MMICs a complete set of measurements must be done. First, to evaluate the circuit parameter dispersion and to perform an initial selection of the chips having a good behavior. Those measurements are usually done on-wafer or on-chip. In order to improve the performance of the selected chips an external network is normally needed. In these cases the chip is mounted on a carrier in which the external devices (chip capacitors, resistances, etc.) are also connected. In some cases noise measurements are preferably done on-carrier. In any case on-carrier measurements are needed to test the dependence with temperature variations. Finally, to evaluate the behavior of the complete system or subsystem in which the MMIC is to be employed, special set-ups are usually required to include the MMIC chip and the rest of the subsystem in an unique package and to optimize at the same time the interconnections between them.
With the aim of being able to perform in a fast and economical way that complete set of measurements over the different MMICs that are being designed at the Polytechnic University of Madrid a test method and several set-ups have been developed. The objective of this paper is two fold. In one hand it presents that method and those test set-ups highlighting their main features. In the other hand it demonstrates that the GaAs monolithic transimpedance amplifier tested following those procedures has excellent performances for low noise and high speed optical communication systems.

2. TESTING FACILITIES

Fig.1 shows part of the testing facilities. Among them it may be mentioned:

a) a Cascade Microtech Summit 9000 analytical probe station. Calibration of the station is performed by means of the calibration substrates provided with it. The station is employed for on-wafer and on-chip DC, RF and noise measurements (see fig.2).

b) an in-house test-fixture (based on Ref.1) specially designed to perform fast on-carrier measurements of the MMICs, particularly important when many chips must be tested. Very good repeatability has been obtained. Its main features are that the input and output microstrip lines of the carrier must not be bonded to the test fixture and no housing of the carrier or connectors are needed. Each chip to be measured is mounted

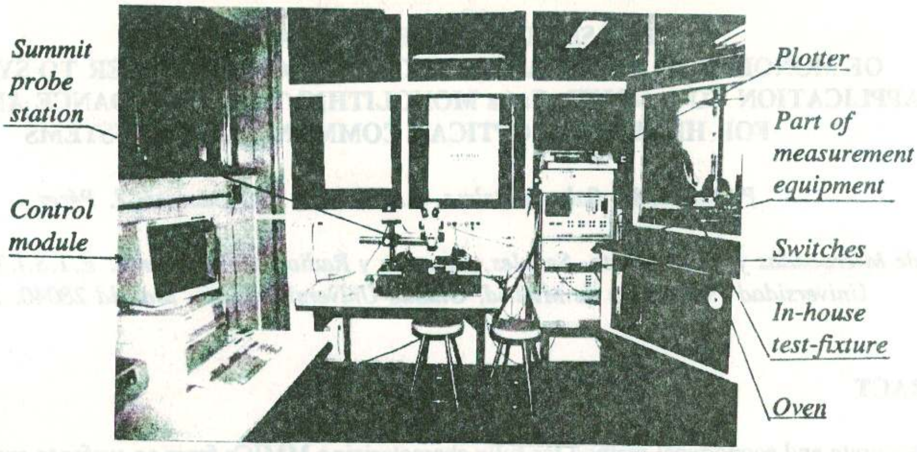


Fig.1. Partial view of the measurement facilities

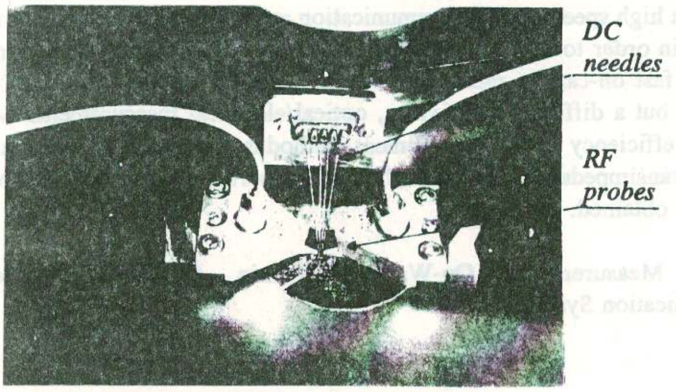


Fig.2. On-wafer measurements

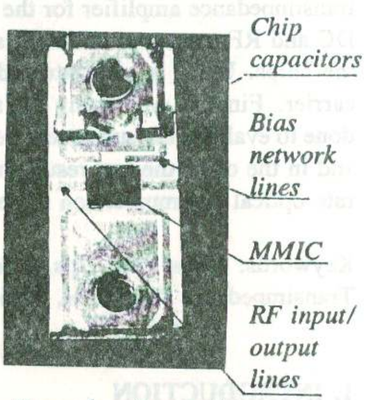


Fig.3. Example of a carrier

on a carrier (see fig.3). The carrier is then placed (just screwing it to the stage, see fig.5) between the contact tips of the test-fixture. These are designed to ensure and excellent contact to the input and output lines of the carrier (see fig.4). Accurate and fast measurements are possible. Special carriers have been designed for calibration purposes (with a trough line, a short circuit, etc.). This test fixture is used for on-carrier DC, RF, noise and temperature dependence measurements (see fig.5). The facilities easily allow measurements from -20^0 to 80^0 C. Means are available for further extensions of those limits.

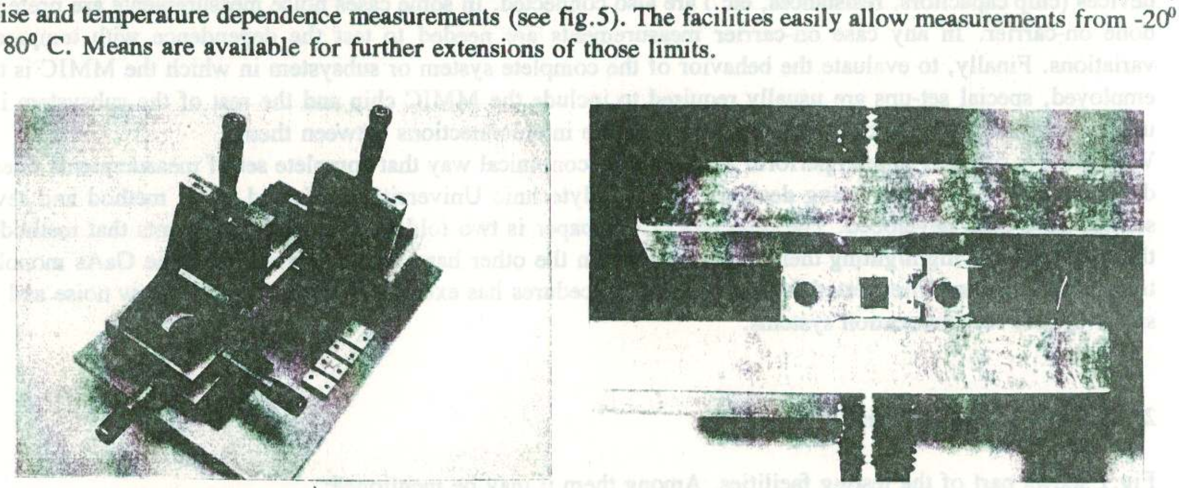

a) b)

Fig.4. In-house test-fixture. a) Test fixture (without the stage). b) Detail of the carrier ant contact tips.

c) the HP 83040 modular microcircuit package, for which extra modules have been fabricated to perform on-carrier system or subsystem measurements. In particular a module has been designed to make compatible the above mentioned carriers with both test fixtures. The carriers are screwed to that module (see fig.6). System measurements are easily performed cascading the carrier modules with the modules supporting

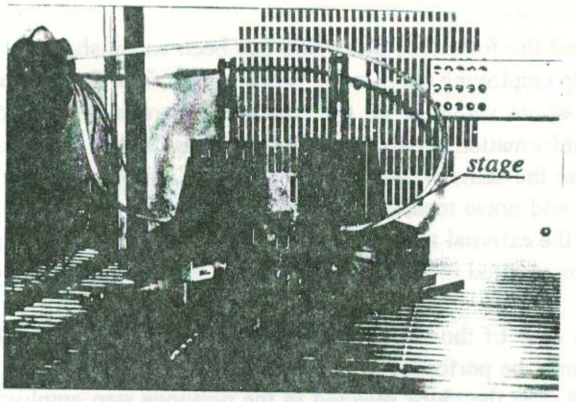


Fig.5. In-house test-fixture inside the oven

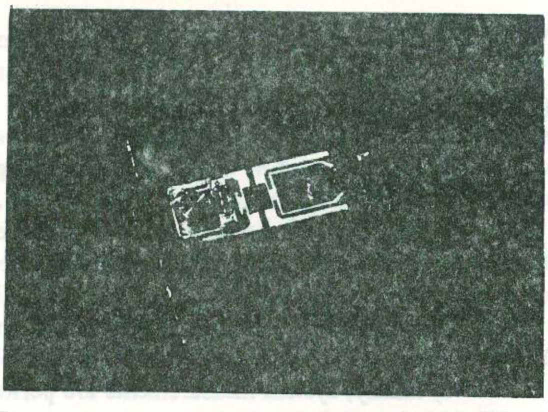


Fig.6. Carrier module for the HP83040 test-fixture

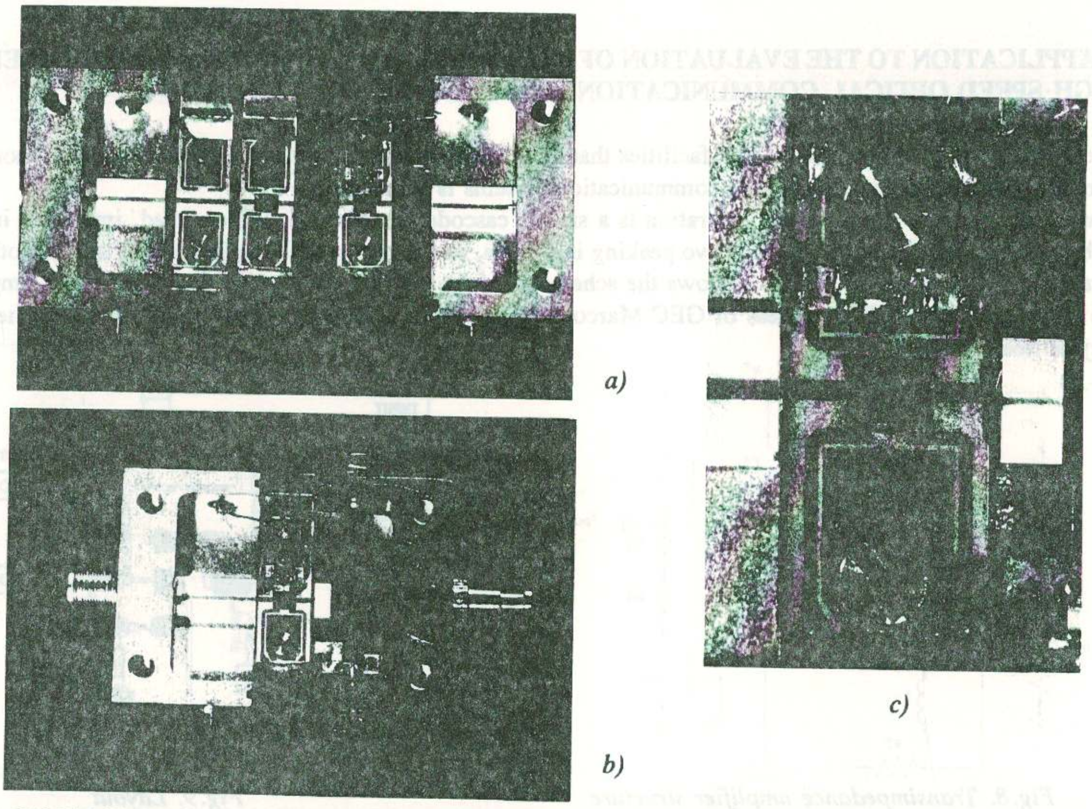


Fig.7. HP 83040 test-fixture and extra modules. a) The modular package, carrier and calibration modules. b) Example of the use of the test fixture for optical/electrical measurements. c) Detail of b) showing the pin diode and the MMIC transimpedance amplifier.

the rest of the system. Obviously, in this case, the input and output microstrip lines of the carrier must be bonded to the lines of the adjacent modules. The calibration of the test-fixture is accomplished employing the same calibration carriers of the in-house test-fixture (see fig.7).

d) the DC, RF and noise measurement equipment (sweep oscillators, network and spectrum analyzers, power meters, power suppliers, etc.) and a panel of switches that allow to automatically commute from the on-wafer set-up to any of the test fixtures.

e) a control module automatically stores the measurements and perform any mathematical or logical function that should be needed. Plotting facilities are provided.

A mechanical workshop is also available in which the carriers, the desired modules and, eventually, the housing are fabricated. The facilities cover from the design step to the final fabrication in thin technology with plastic and ceramic substrates. Means for precise bonding are also available.

3. MMIC TESTING PROCEDURE

When a high number of chips of a MMIC must be tested the following procedure has been established:

a) the chips are firstly tested on-wafer or on-chip employing the Summit probe station. The DC working point is optimized for one of the chips and then the whole wafer or all the diced chips are measured in a straightforward way. These measurements will provide information about the dispersion across wafer, when they are performed over a whole wafer or chips belonging to the same wafer, and, in any case, they will allow to discard the chips having a incorrect behavior. DC, RF and noise measurements are possible.

b) a carrier is designed that provides space for the external network and the bonding pads for the wires for the interconnections to the power suppliers. The chips selected in the previous step are mounted each of them on a carrier and bonded to the carrier microstrip lines.

c) the in-house test-fixture is employed to test each of those chips optimizing its working point. DC, RF, noise and temperature dependence measurements may be performed.

d) finally, system measurements are performed over the chips selected in the previous step employing the HP 83040 modular package.

4. APPLICATION TO THE EVALUATION OF A GaAs MMIC TRANSIMPEDANCE AMPLIFIER FOR HIGH SPEED OPTICAL COMMUNICATION SYSTEMS

The application of the procedure and facilities that have been outlined in order to evaluate a GaAs monolithic transimpedance amplifier for optical communication systems is presented.

The transimpedance amplifier configuration is a simple cascode one (Ref.2), DC coupled, improved in terms of bandwidth and noise by means of two peaking inductors, one in series with the input FET and the other one as a series feedback (Ref.3). Fig.8 shows the schematic of the circuit. The device was constructed employing the GaAs half-micron F20 process of GEC Marconi Materials & Technology Limited (GMMTL). The layout may be seen in fig.9.

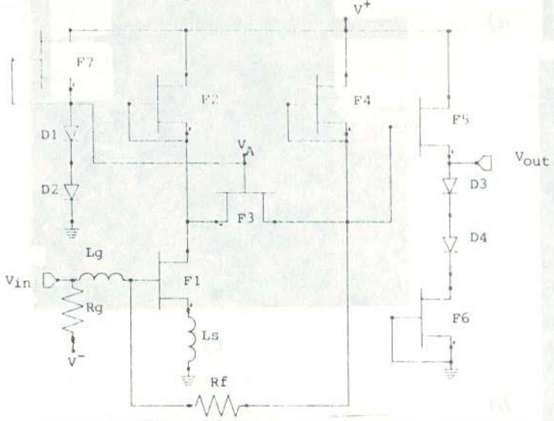


Fig.8. Transimpedance amplifier structure

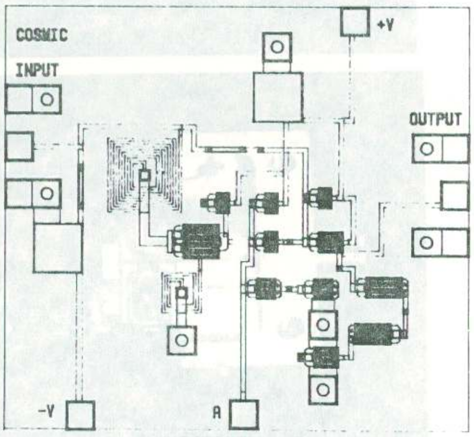


Fig.9. Layout

18 samples of a whole wafer were tested on-wafer, performing DC and RF (S parameters and transimpedance gain) measurements. Fig.10 shows DC and transimpedance gain results. Close agreement with simulation and negligible dispersion across wafer are observed. 14 diced chips of a second wafer were also tested on-chip. The results agrees with the previous ones demonstrating a insignificant dispersion from wafer to wafer.

Several diced chip were tested on-carrier employing the first test-fixture. The working point was optimized in terms of transimpedance gain and bandwidth. DC, RF (S parameters and transimpedance gain) and noise measurements were performed. The bias-point and temperature dependence were tested. Fig.11 shows the low-frequency (200 MHz) transimpedance gain and bandwidth dependence with the bias-point variations for one of the chips. A negligible dependence has been obtained, with a transimpedance gain of about 63.5 dBΩ, a bandwidth from DC to 1.7 GHz and a power consumption of 0.53 W. Fig.12 shows the test set-up for the equivalent noise current measurements. Fig.13 shows that an equivalent noise current of about 5 $pA/\sqrt{Hz}$ has been obtained in close agreement with simulations. Figs.14 and 15 show DC, S parameters, transimpedance gain and noise results for six different values of the temperature. The dependence is again insignificant.

Finally optical/electrical measurements were performed using the HP83040 modular package. Fig.7 shows the

$V^{+}\equiv 7(v)$; $V^{-}\equiv -6(v)$;	$P_C = 590$ (mW)
$\overline{I}^{+} = 83.43$ (mA)	$\sigma_{I^+} = 3.02$ (mA)
$\overline{I}^{-} = 1.80$ (mA)	$\sigma_{I^-} = 0.01$ (mA)

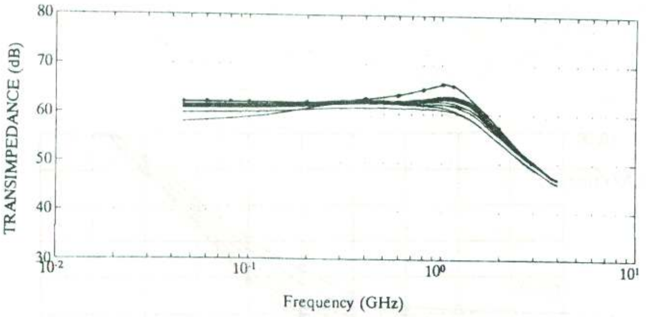


Fig.10. On-wafer DC and transimpedance gain results for 18 samples. • Simulation.

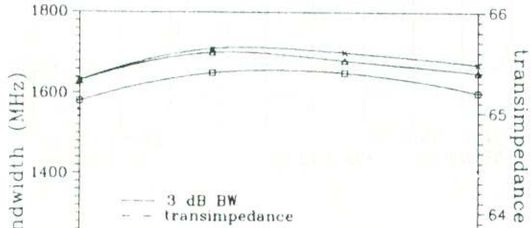
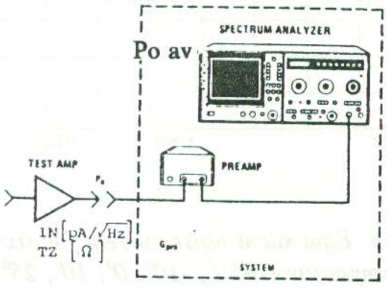


Fig.11. Bias-point dependence (on-carrier)



$$P_{o\,av}\,[\mathrm{mW/Hz}] = P_{o\,av}\,[\mathrm{mW}]\,/\,BW\,[\mathrm{Hz}],\quad [\mathrm{mW/Hz}]$$

$$P_o\,[\mathrm{mW/Hz}] = P_{o\,av}\,[\mathrm{mW/Hz}]\,/\,G_{pre}$$

$$P_o\,[\mathrm{dBc}] = 10\log(P_{o\,av}\,[\mathrm{mW}]) - 10\log(BW[\mathrm{Hz}]) - 10\log(G_{pre})$$

$$V_N^{rms}(f) = (P_o[\mathrm{W/Hz}].Z_o[\Omega])^{1/2},\quad [\mathrm{V}/\sqrt{\mathrm{Hz}}]$$

$$I_{NC}^{rms}(f) = \frac{V_N^{rms}(f)\,[\mathrm{V}/\sqrt{\mathrm{Hz}}]}{|TZ(f)|\,[\Omega]},\quad [\mathrm{pA}/\sqrt{\mathrm{Hz}}]$$

Fig.12. Test set for equivalent noise current measurement

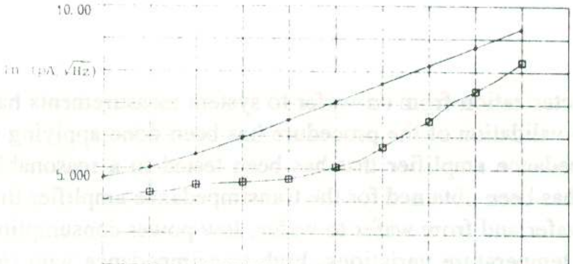
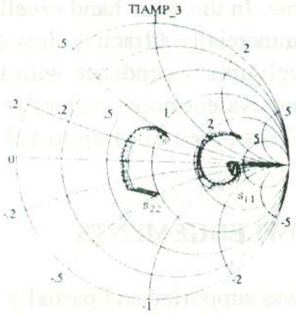


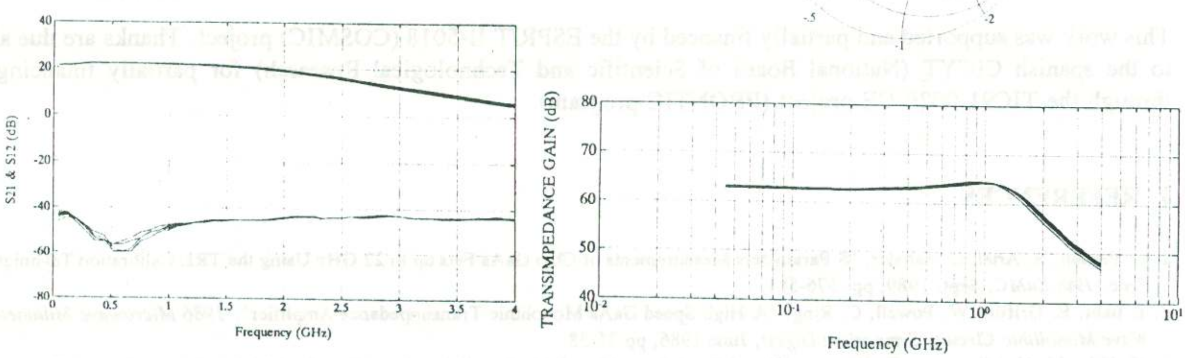
Fig.13. Equivalent noise current for an on-carrier chip. • Simulation.

$V^{+} = 7$ (v),	$V^{-} = -5.5$ (v)					
Tempt.	-20°	-10°	0°	10°	25°	50°
I^{+}(mA)	79	78	78	77	74	73
I^{-}(mA)	1.8	1.8	1.8	1.8	1.8	1.8
P_C(mW)	563	556	556	549	528	521

a)



b)



c) *d)*

Fig.14. Temperature dependence for an on-carrier chip. a) DC. b) S_{11}, S_{22}. c) S_{12}, S_{21}. d) Transimpedance gain.

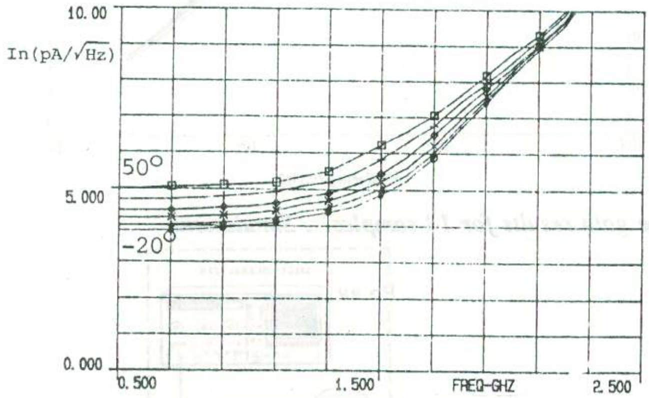


Fig.15. Equivalent noise current for six values of the temperature (-20⁰, -10⁰, 0⁰, 10⁰, 25⁰, 50⁰ C)

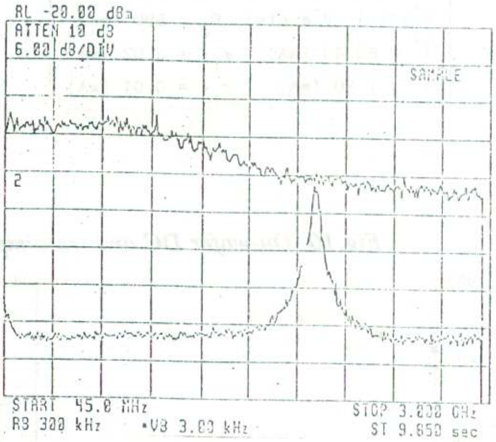


Fig.16. Optical/electrical results with an EPITAXX InGaAs PIN photodiode of 0.1 pF

assembly in which the photodetector employed (an EPITAXX high speed back-illuminated InGaAs PIN photodiode of 0.1 pF mounted on a ceramic substrate) may be seen. Fig.16 gives results for one chip, showing a bandwidth from DC to 1.35 Ghz. Assuming a roll of factor of 0.8 the transimpedance amplifier will allow speed rates up to 1.7 Gb/s.

It is the authors opinion that thanks to the use of the above mentioned method the characterization of all those chips was completed not only in an economical way but in a reasonable period of time.

5. CONCLUSIONS

A method for MMIC fast, accurate and economical characterization from on-wafer to system measurements has been outlined. The test set-ups have been presented. The validation of the procedure has been done applying it to the evaluation of an enhanced GaAs MMIC transimpedance amplifier that has been tested in a reasonable period of time. In the other hand excellent performances has been obtained for the transimpedance amplifier that makes it commercially attractive: low dispersion across wafer and from wafer to wafer, low power consumption (0.5 W), negligible dependence with the bias-point and temperature variations, high transimpedance gain (63 dBΩ), low equivalent noise current (5 pA/√Hz), and a wide transimpedance-gain bandwidth from DC to 1.7 GHz that allows speed rates up to 1.7 Gb/s, when a PIN photodiode of 0.1 pF is employed.

6. ACKNOWLEDGEMENTS

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