Design of a Ka band Power Amplifier for Phased Array Antennas in GaN technology

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***Abstract* — This paper presents the design of a multistage power amplifier within the project "*Development of electronic circuits based on customized MMICs for shaping a beam in advanced radar and communications systems*". The amplifier is designed using GaN D01GH technology from OMMIC. The amplifier has been designed using Pathwave Advanced Design System (ADS) software and operates in Ka band (27.5-30 GHz).**

Keywords-component; Power Amplifier, Amplifier, Single Stage, Multistage, Stage, Maximum Power, Maximum Gain, Adaptation Networks, Schematic, Layout, Transistor.

I. INTRODUCTION

The required specifications of the power amplifier are shown in Table I. This amplifier is situated just before the patch antenna in a phased array for satellite communications.

TABLE I. POWER AMPLIFIER TO BE DESIGNED.

Initial specifications	
Frequency range	27.5 – 30 GHz
Small signal gain	20 dB
Large signal gain	20 dB
Input matching (S11)	< –10 dB
Output matching S22)	< –10 dB
PAE	Maximum
Saturation power at 5 dB compression	25 – 30 dBm
Power consumption at 5 dB compression point	The smallest possible

II. DESIGN OF A SINGLE STAGE POWER AMPLIFIER

The manufacturer's recommendations were followed to bias the transistor. A drain (VDS) voltage of 12 V and a gate source voltage of -1.75 V have been used to bias the transistor, so the amplifier is working in AB class. The single stage power amplifier is shown in Figure 1.

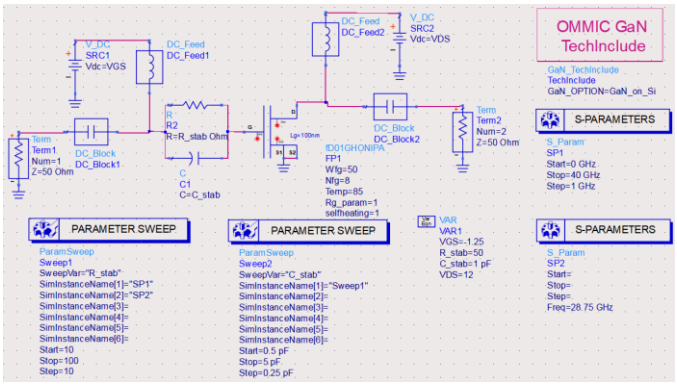

Figure 1. Schematic of the transistor with the stabilization network.

The next step is to find the source and load impedance of this transistor to obtain the maximum power (see Figure 2).

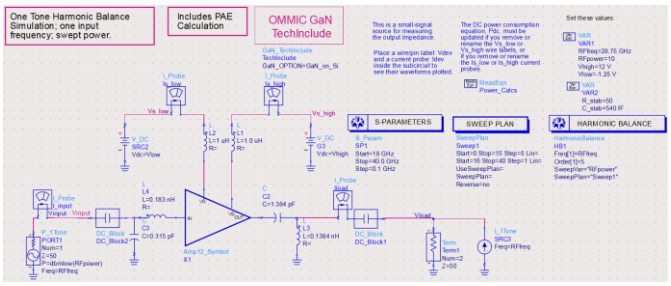

Figure 2. Single-stage power amplifier for maximum power.

Afterward, the single stage amplifier was matched for maximum gain, see Figure 3.

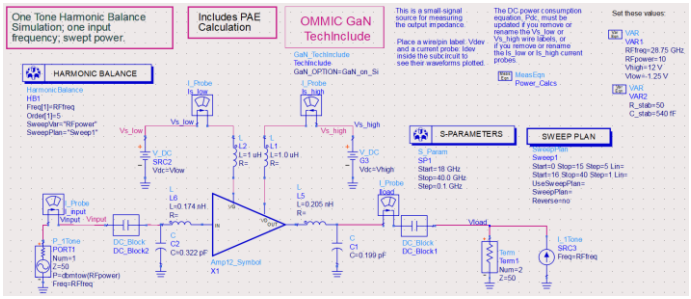

Figure 3**.**Single-stage power amplifier for maximum gain.

Table II shows a comparison of the different single stage amplifiers.

TABLE II. COMPARISON OF THE DIFFERENT SINGLE STAGE AMPLIFIERS

Amplifier for:	Gain	PAE	P_{SAT} a 5 dB
Maximum power	8.4 dB	53.7 %	31.193 dBm
Maximum gain	8.6 dB	52.3 %	31,481 dBm

III. DESIGN OF A MULTISTAGE POWER AMPLIFIER

It has been decided that the best option for the design is a three-stage amplifier. The first two stages are matched for maximum gain and the third are a parallel of two stages matched for maximum output power. The final layout and schematic are shown in Figure 4 and Figure 5, respectively.

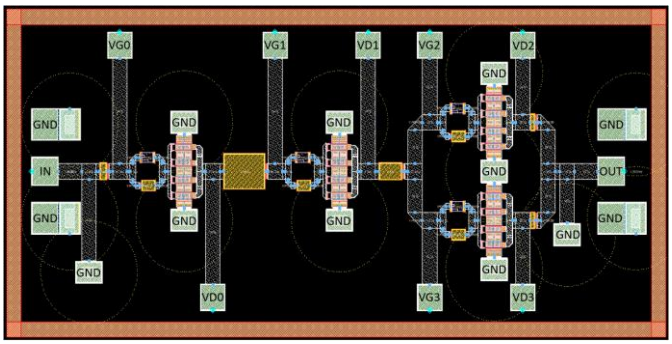

Figure 4. Final layout of the design.

IV. CONCLUSIONS

As can be seen in Table III, the project objectives have been met except for the output matching at central and high frequencies. A good compromise has been reached between all the required specifications. However, the matching of the output could be improved by degrading some other parameter of the amplifier, such as gain or drive power.

TABLE III. COMPARISON BETWEEN INITIAL SPECIFICATIONS AND RESULTS OBTAINED (TYPICAL VALUES)

	Initial specifications	Results obtained (**Typical** values) **@85°C**		
Frequency	27.5 – 30 GHz	27.5 GHz	28.75 GHz	30 GHz
Small signal gain (SP)	20 dB	22.2 dB	21.16 dB	20,04 dB
Big signal gain (HB)	20 dB	22.1 dB	20.96 dB	20.02 dB
Input adaptation (S11)	< –10 dB	–12.5 dB	–14.9 dB	–15.9 dB
Output adaptation (S22)	< –10 dB	–12.5 dB	–8.7 dB	–6.63 dB
Maximum PAE	Maximum	27.15 %	21.94 %	17.76 %
Saturation power at 5 dB compression	25 – 30 dBm	34.02 dBm	33.19 dBm	32.82 dBm
Power consumption in 5 dB compression point	The smallest possible	10 W	10,5 W	11,5 W

References

[1] "OMMIC | Innovating with III – V's", Ommic.com. [Online]. Available: https://www.ommic.com/. [Accessed: 20- Mar- 2021].

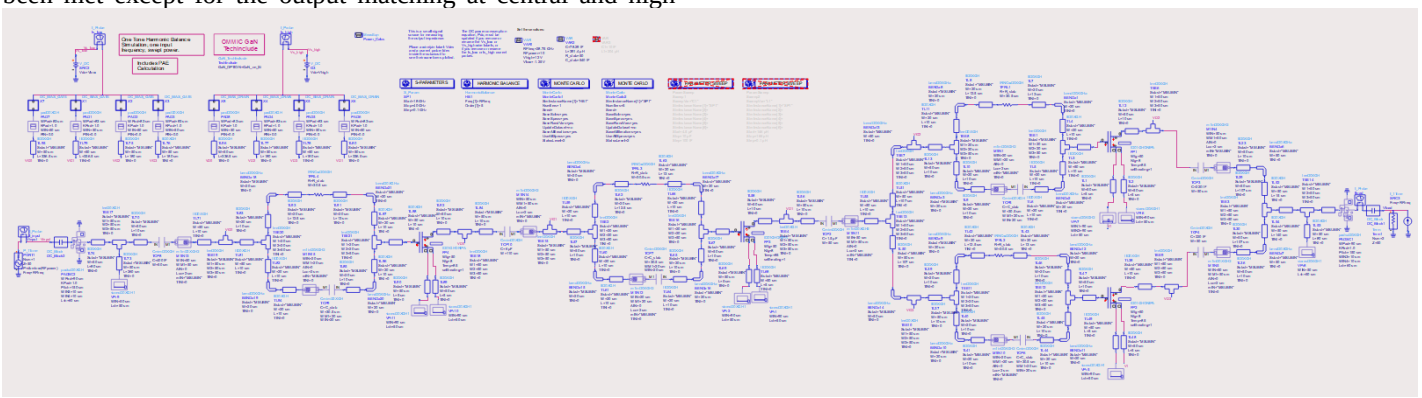

Figure 5. Final schematic design.